

FIG. 28

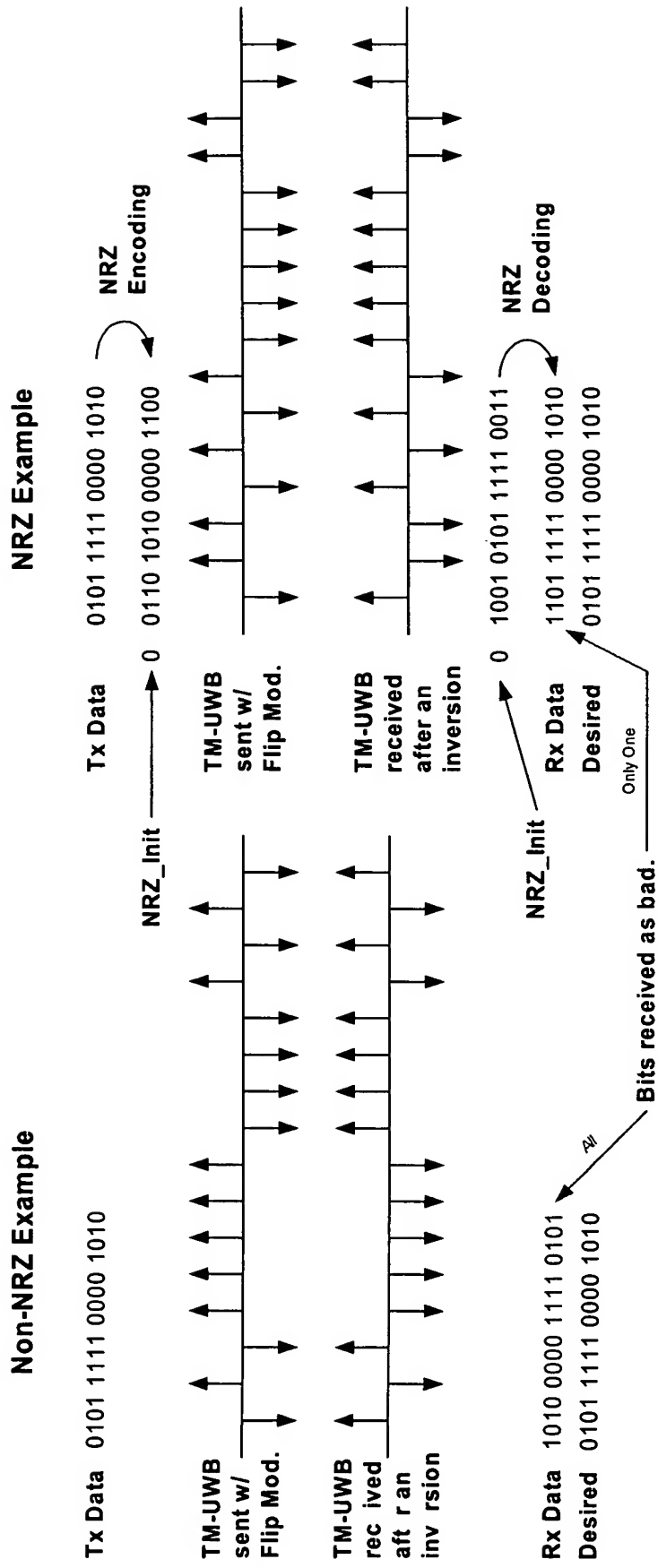


FIG. 29

Timer Control Logic Simplified Block Diagram

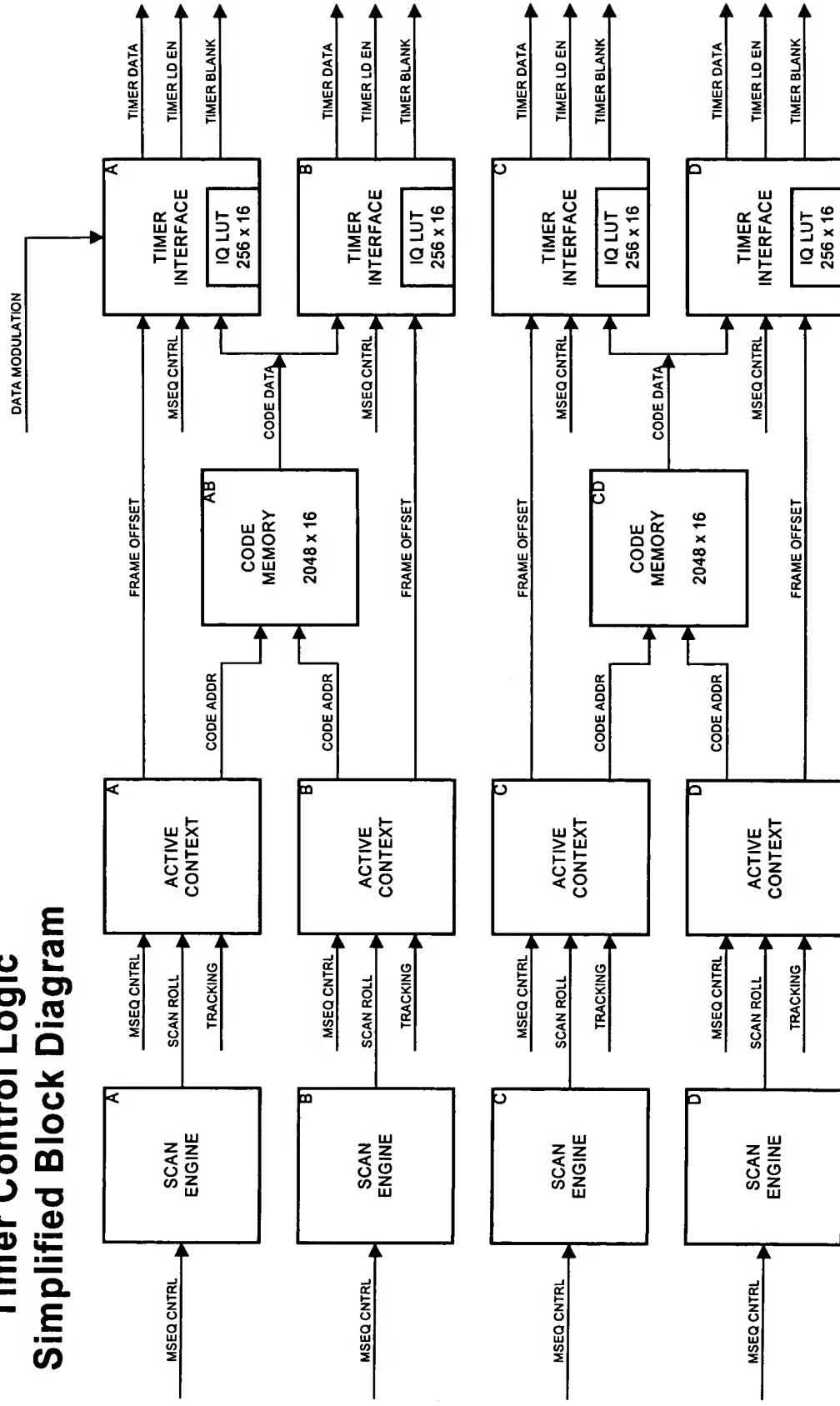


FIG. 30

[illegible]

FIG. 31

[illegible]

CONTEXT SAVE/RESTORE MUXING

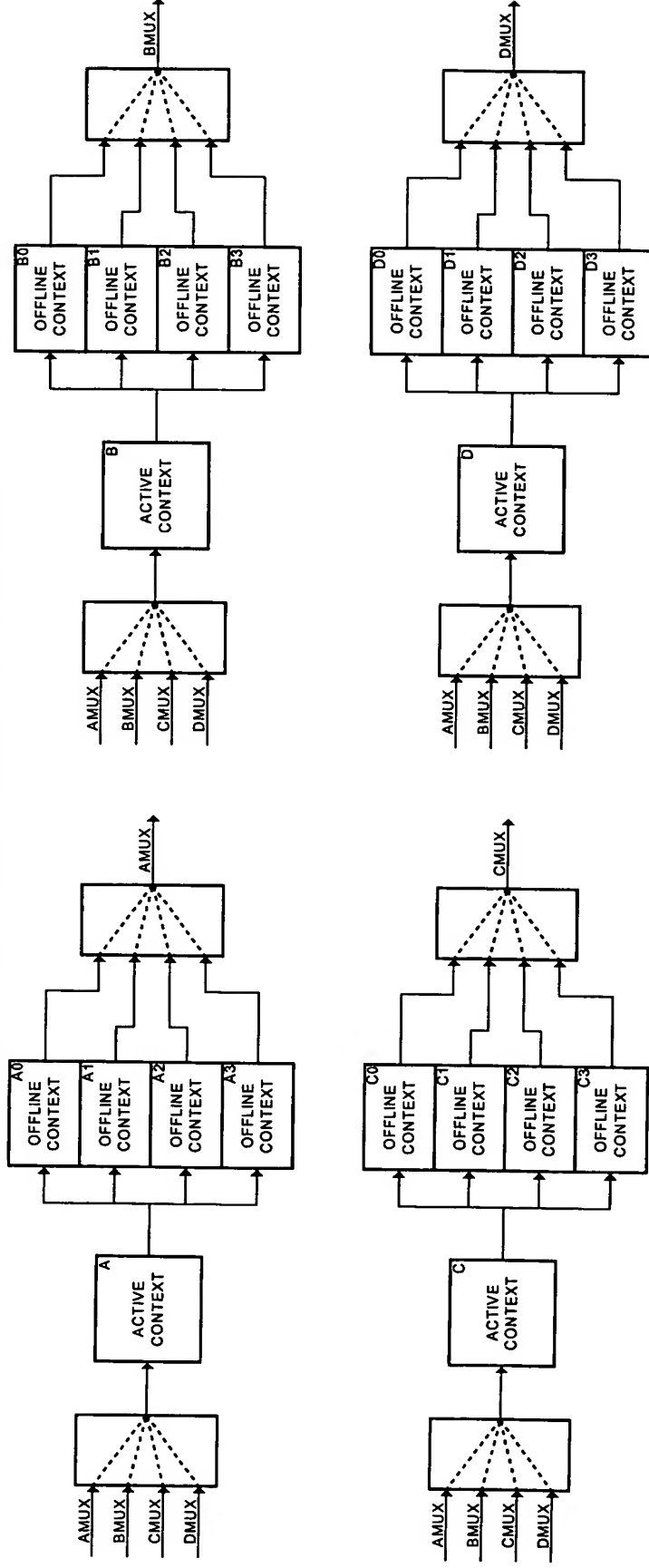


FIG. 33

[illegible]

FIG. 34

[illegible]

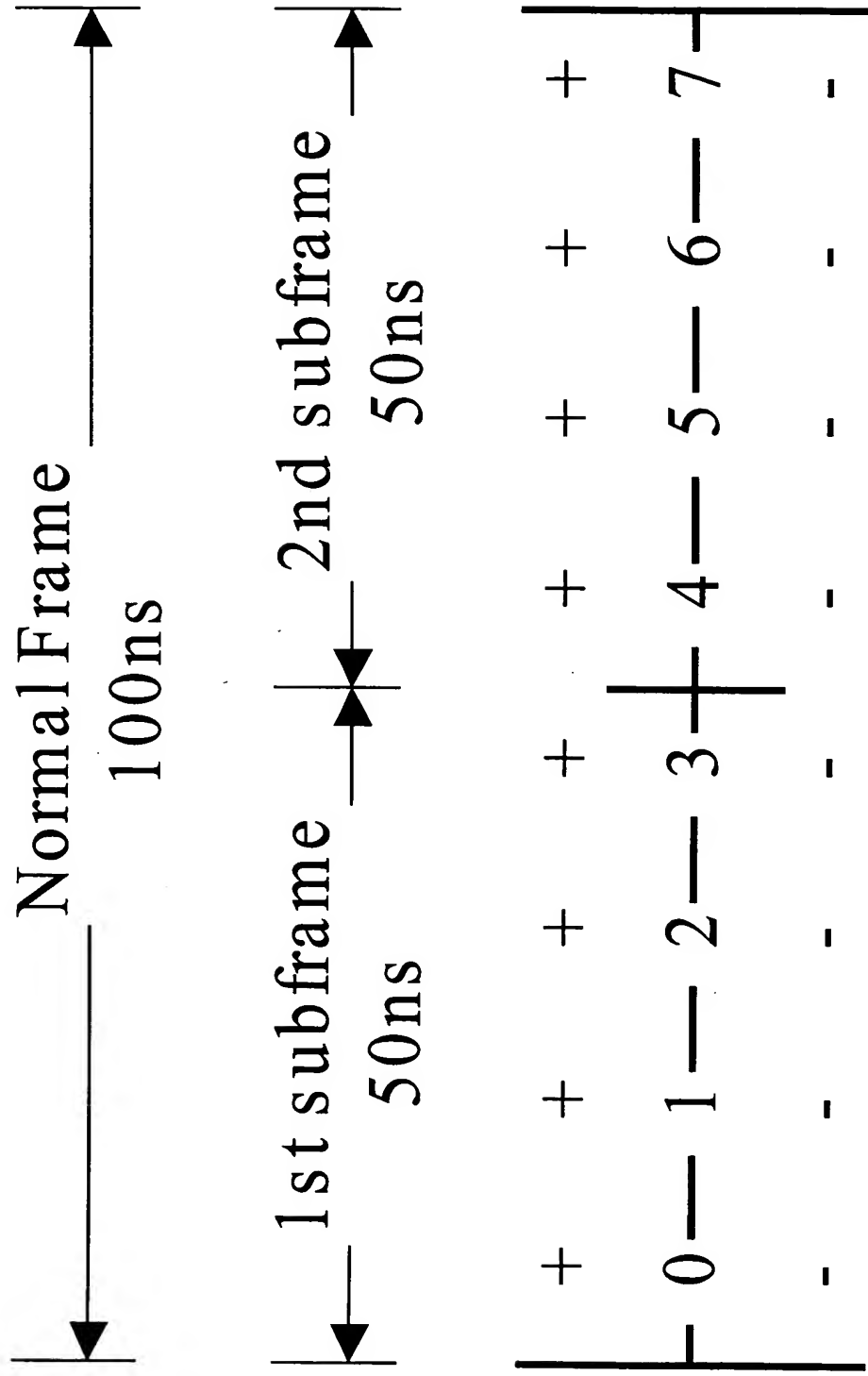


FIG. 36

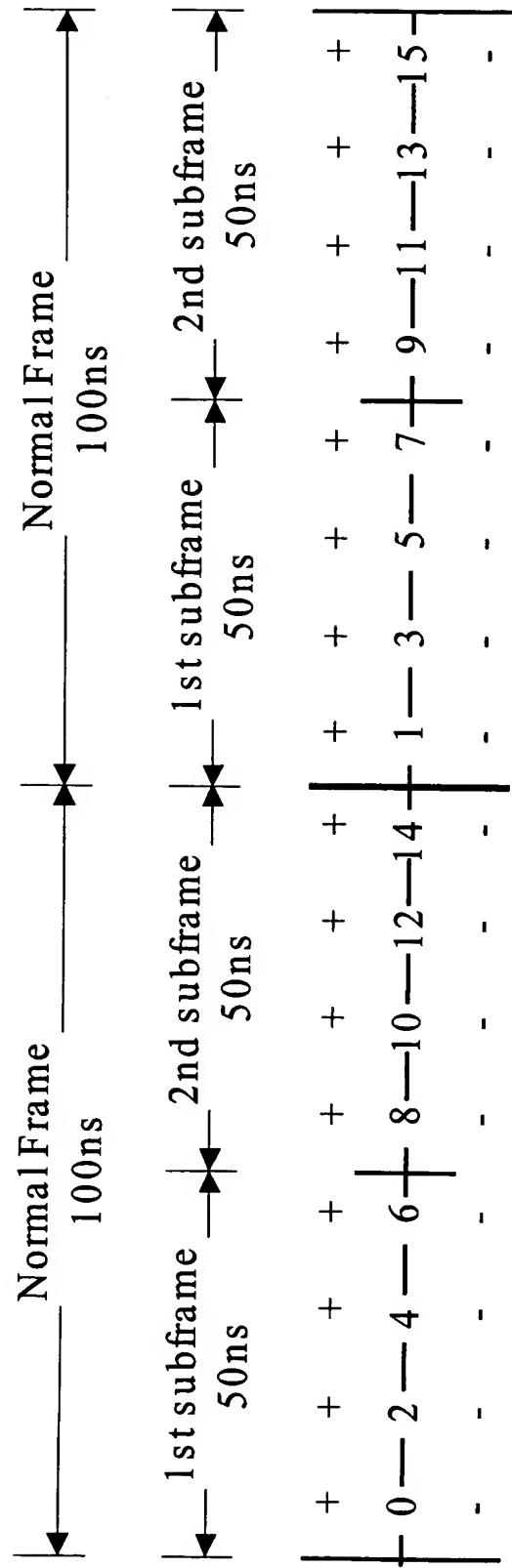


FIG. 37

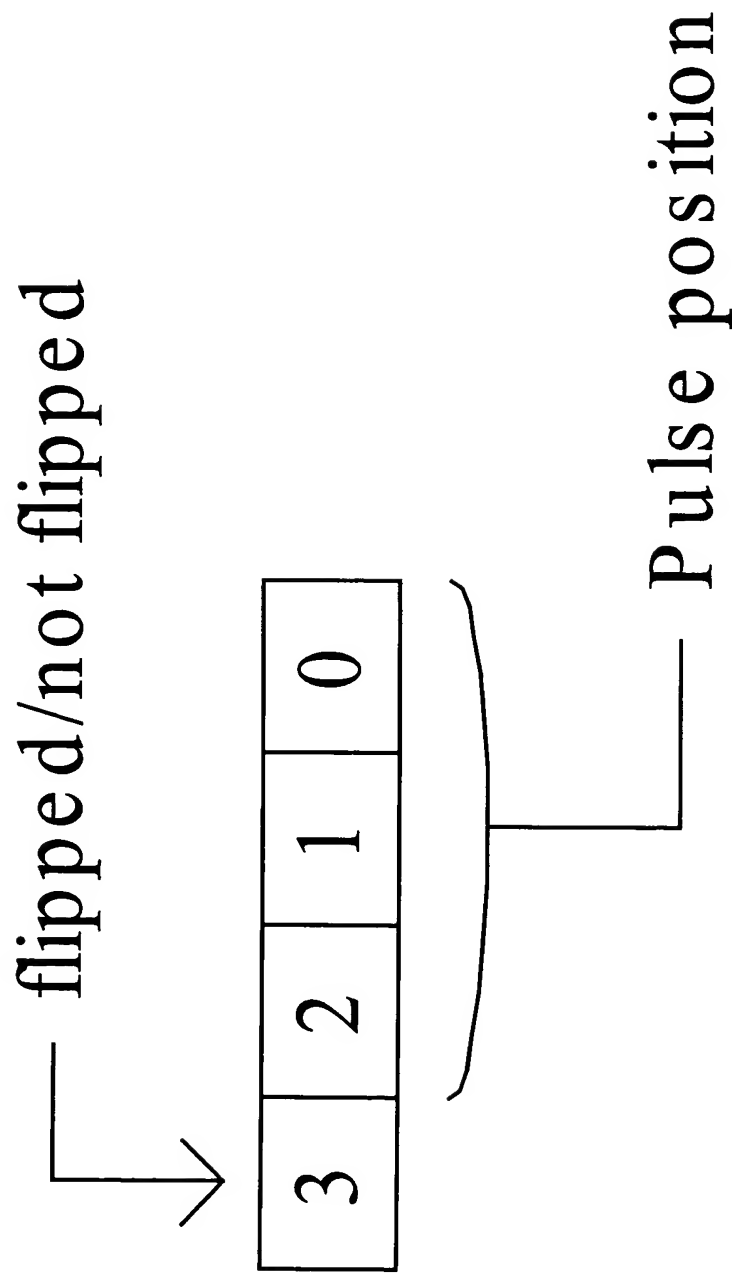


FIG. 38

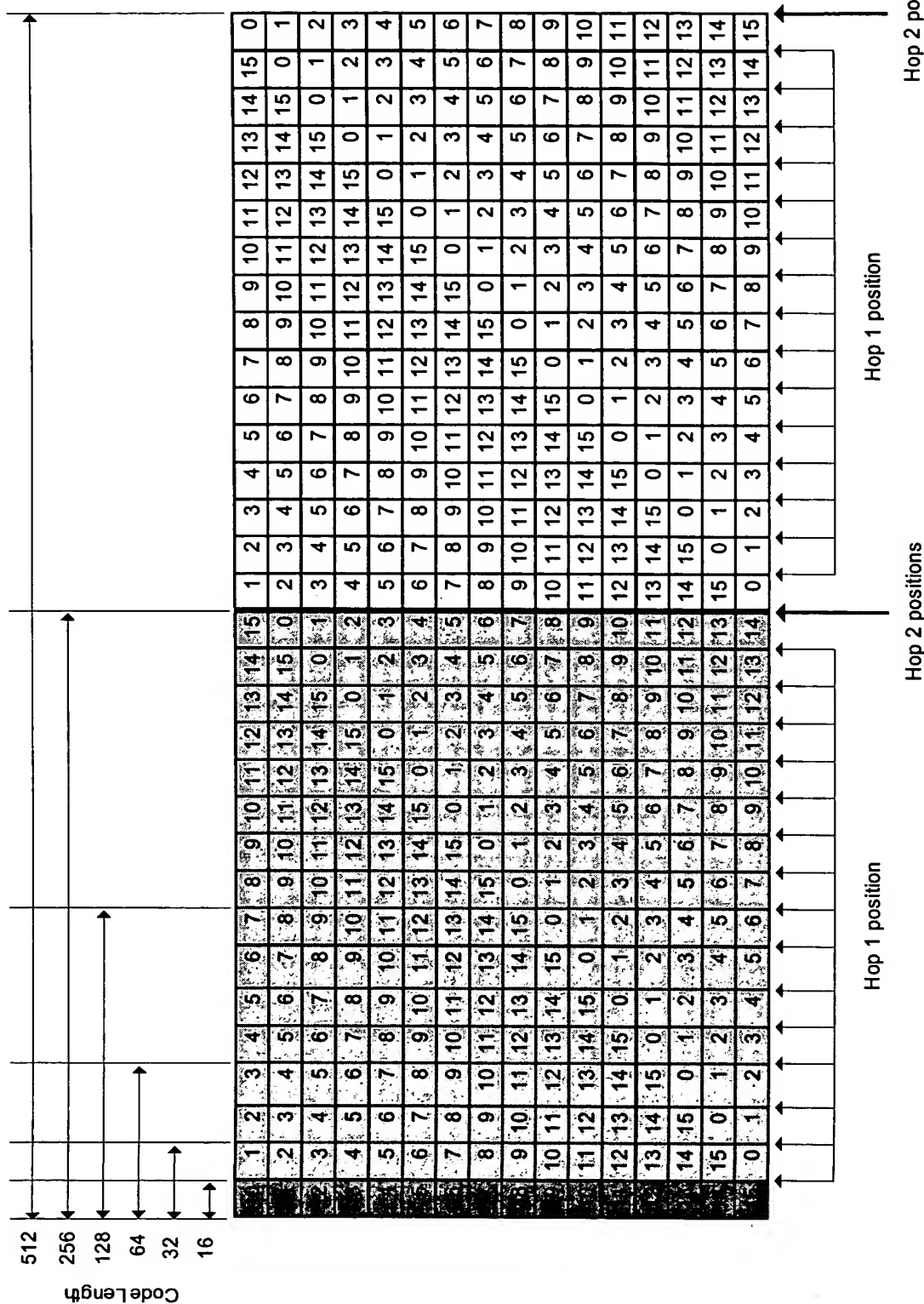


FIG. 39

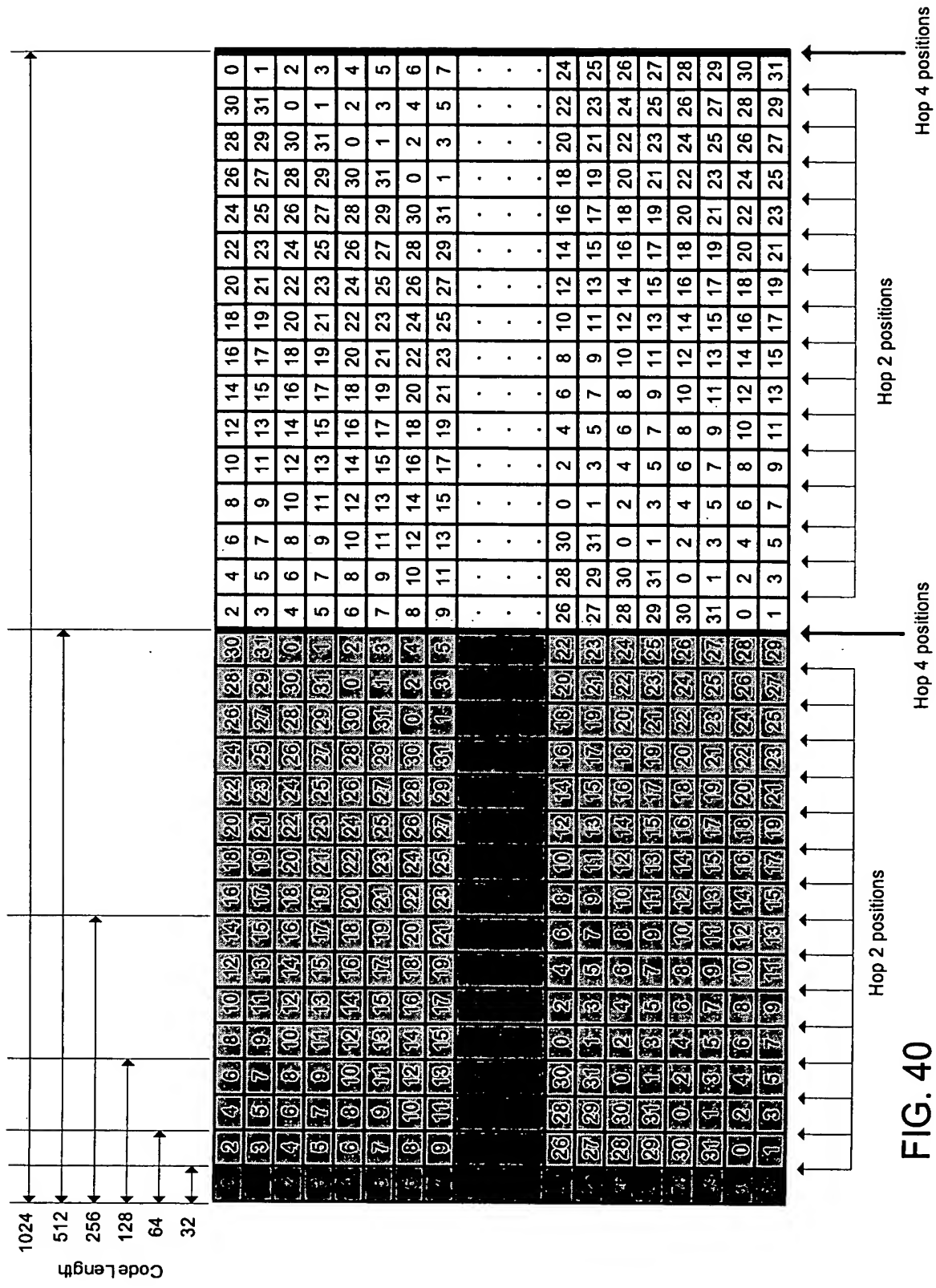


FIG. 40

Ramps built from length 16 code

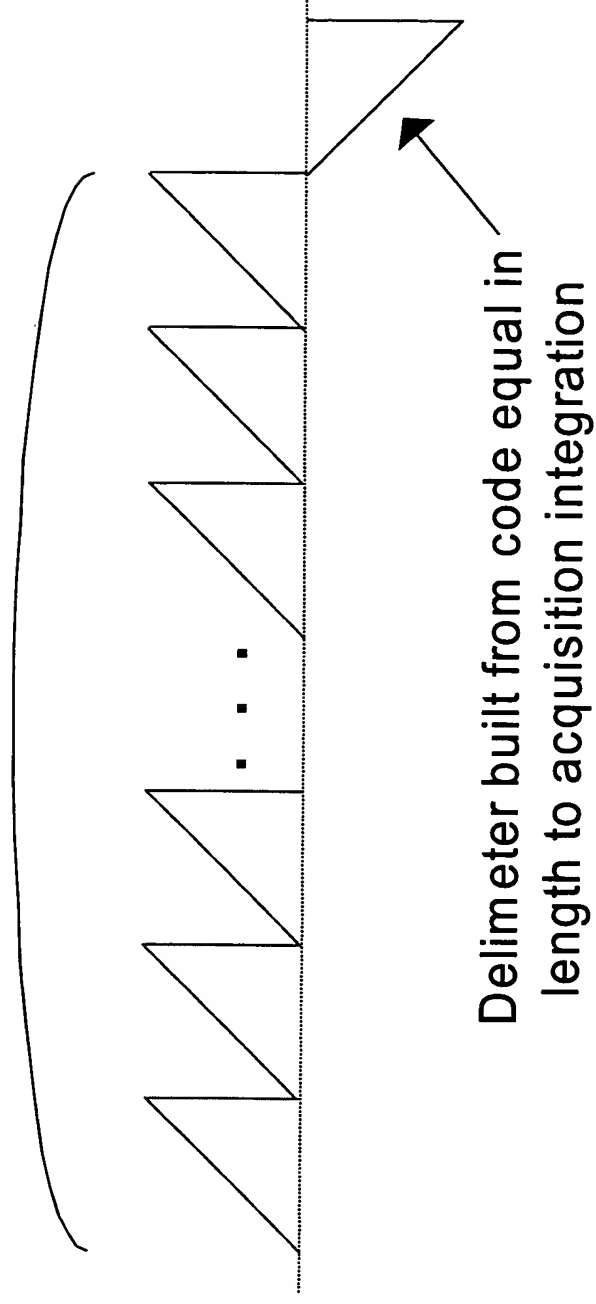
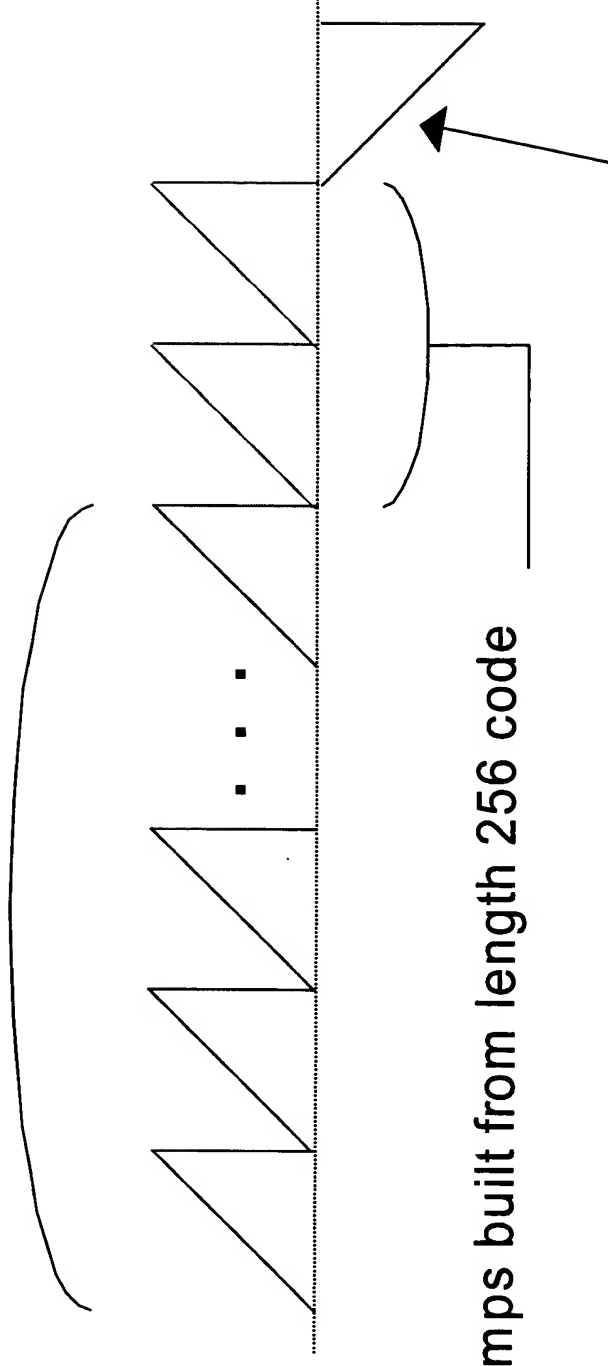


FIG. 41

Ramps built from length 16 code



Delimiter built from code equal in
length to acquisition integration

FIG. 42

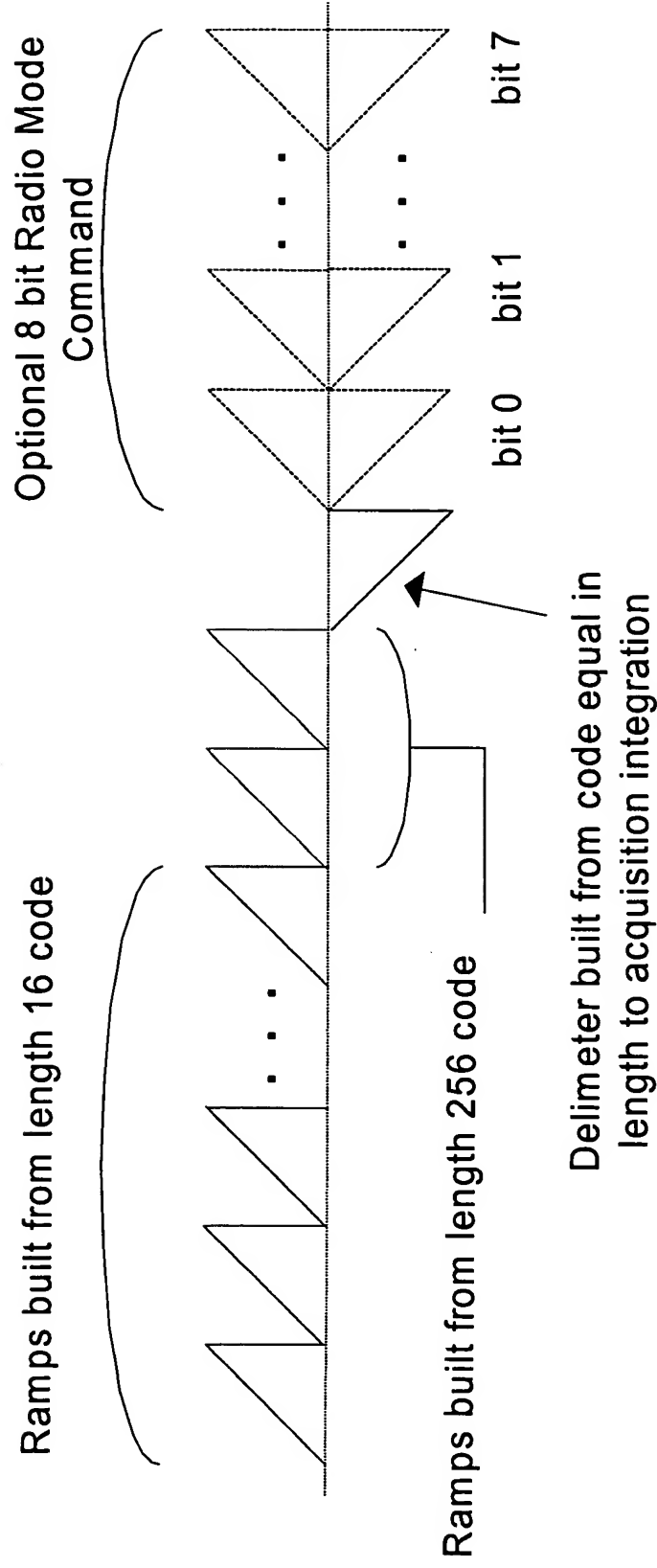


FIG. 43

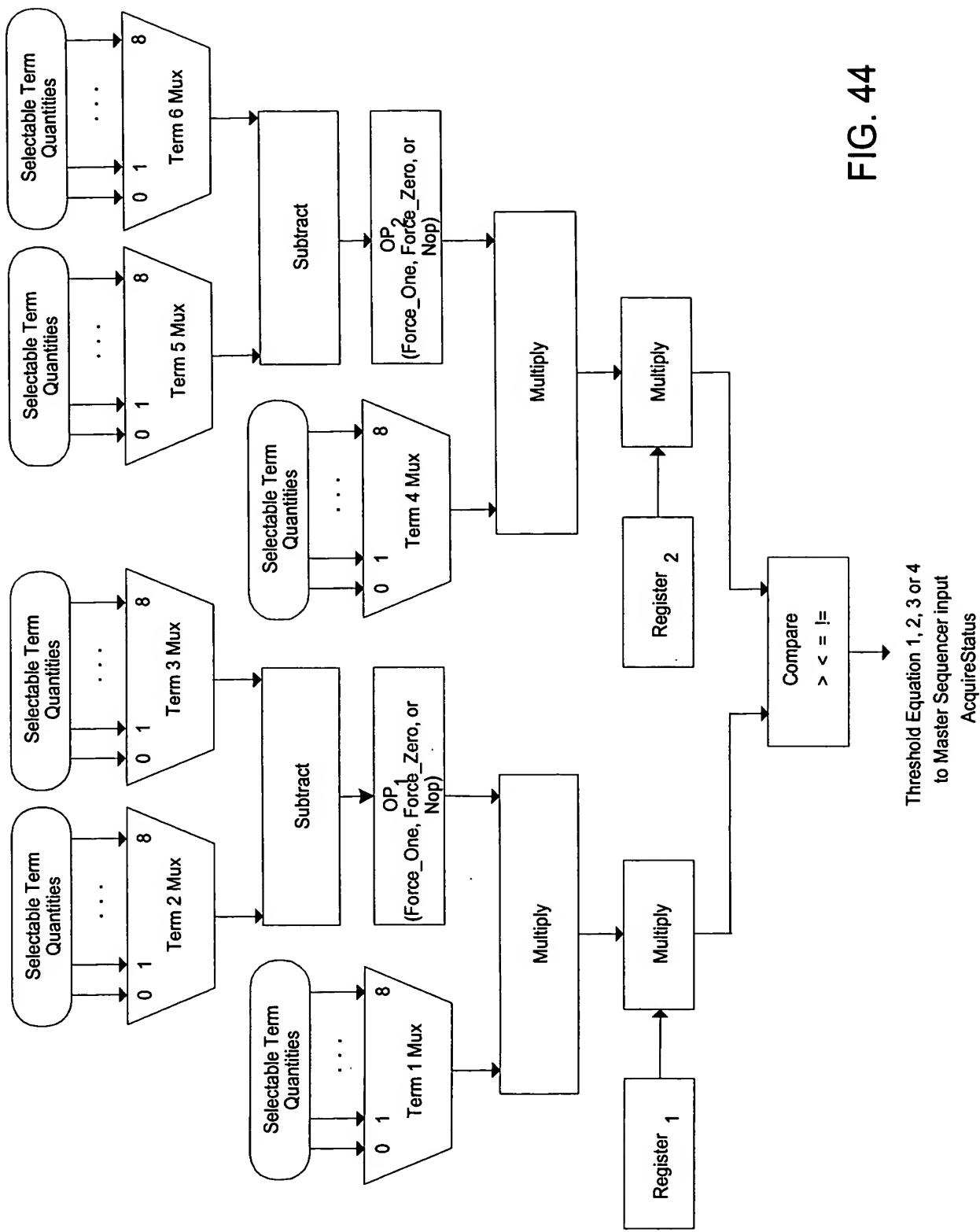


FIG. 44

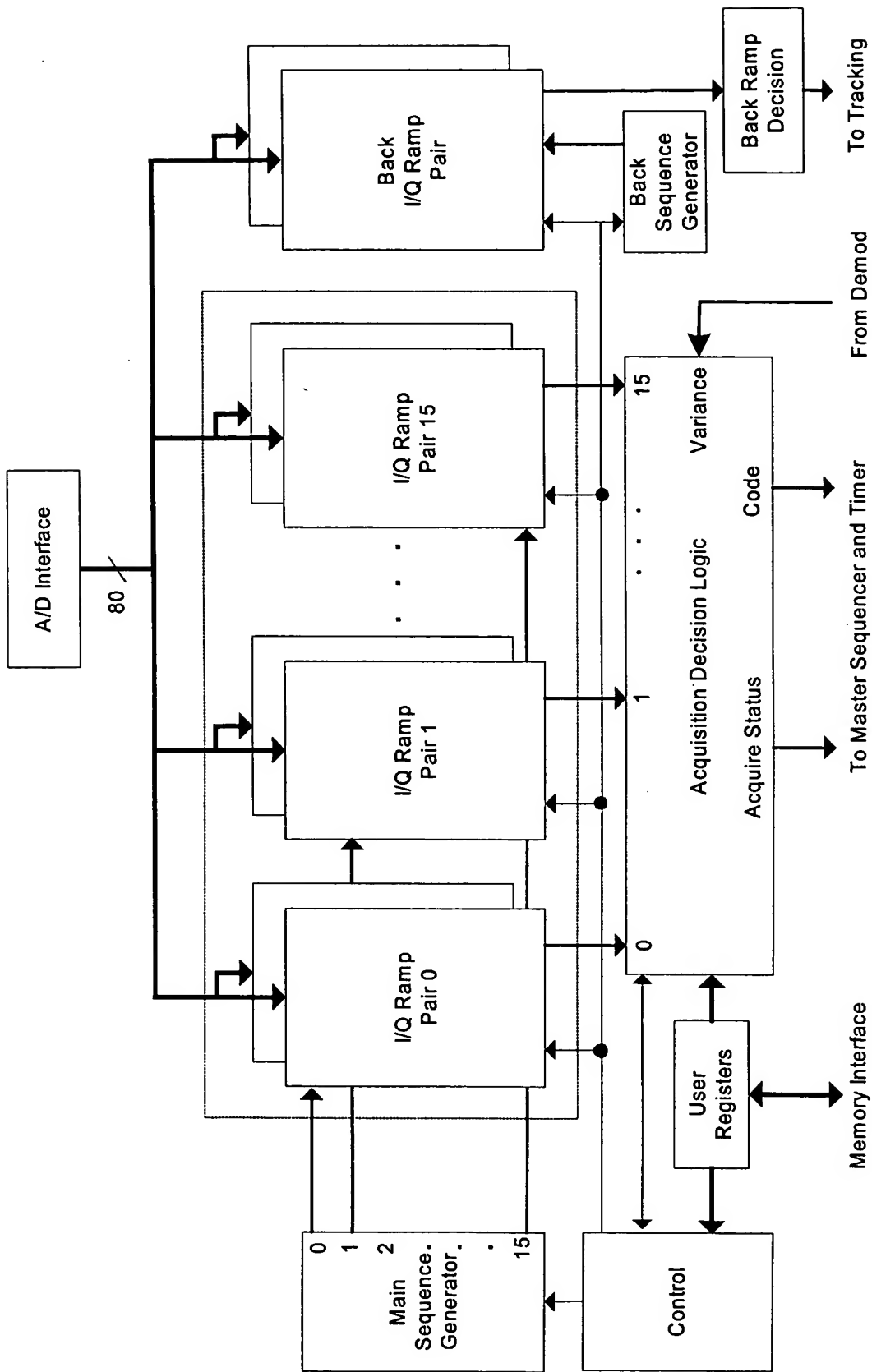


FIG. 45

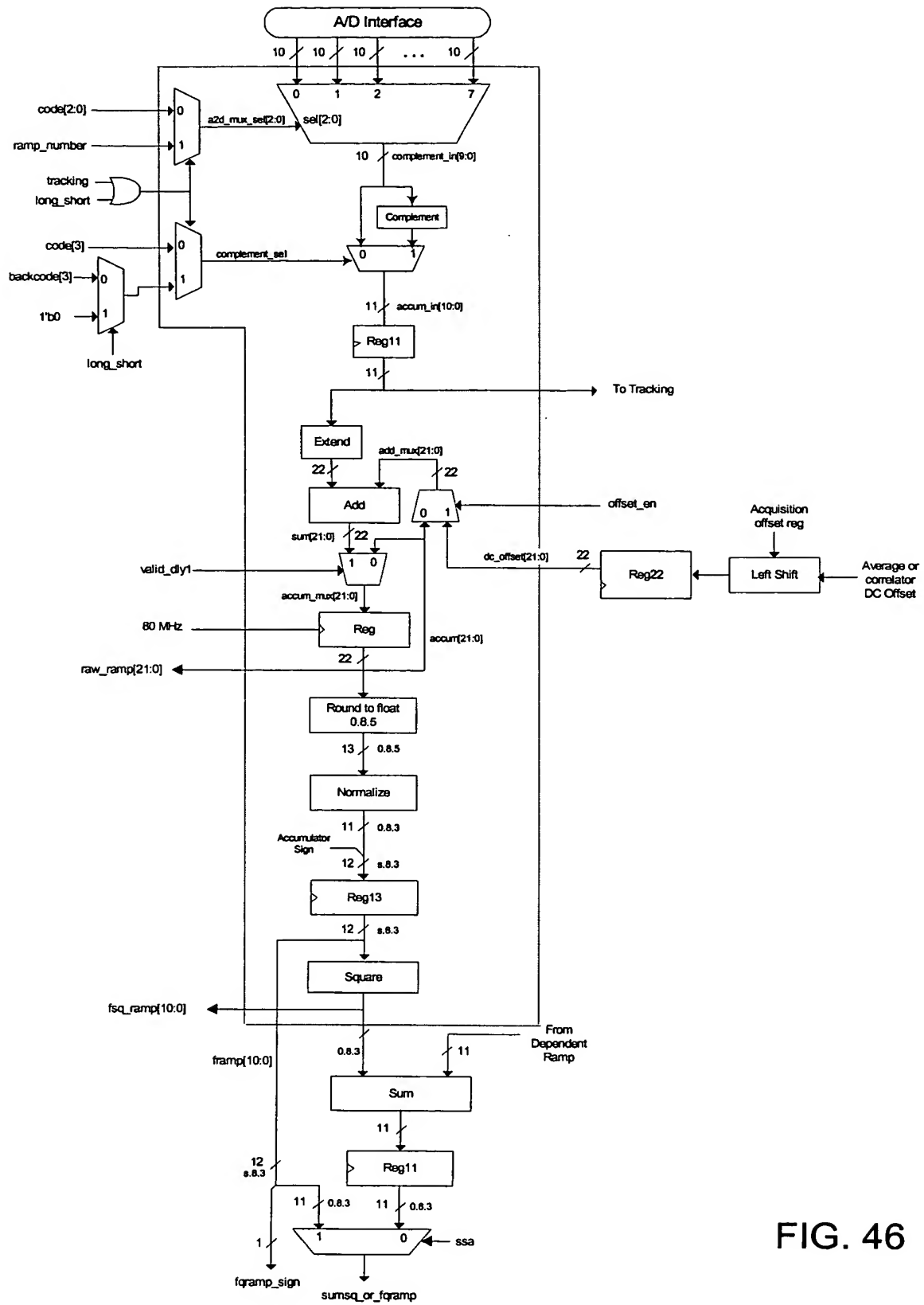


FIG. 46

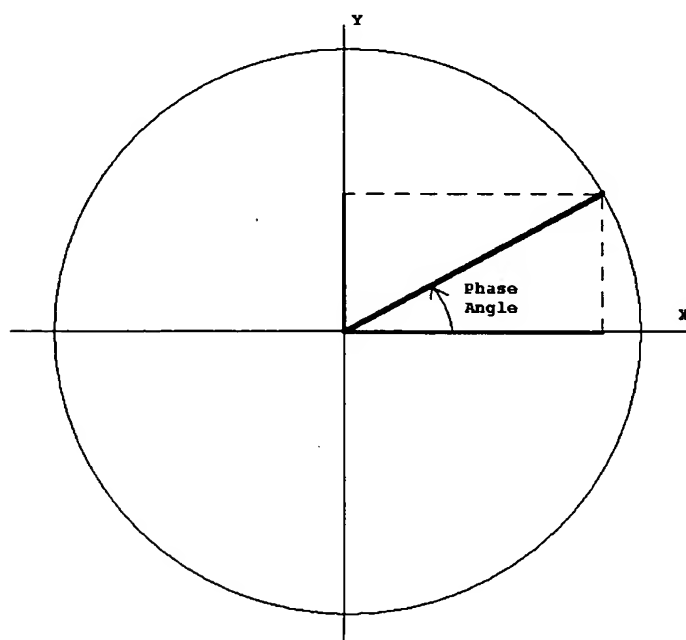
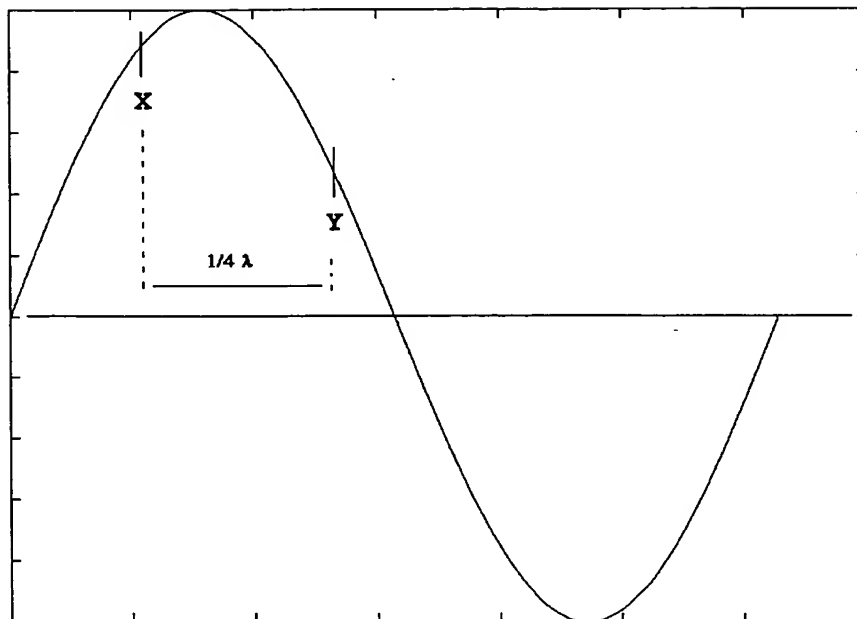


FIG. 47

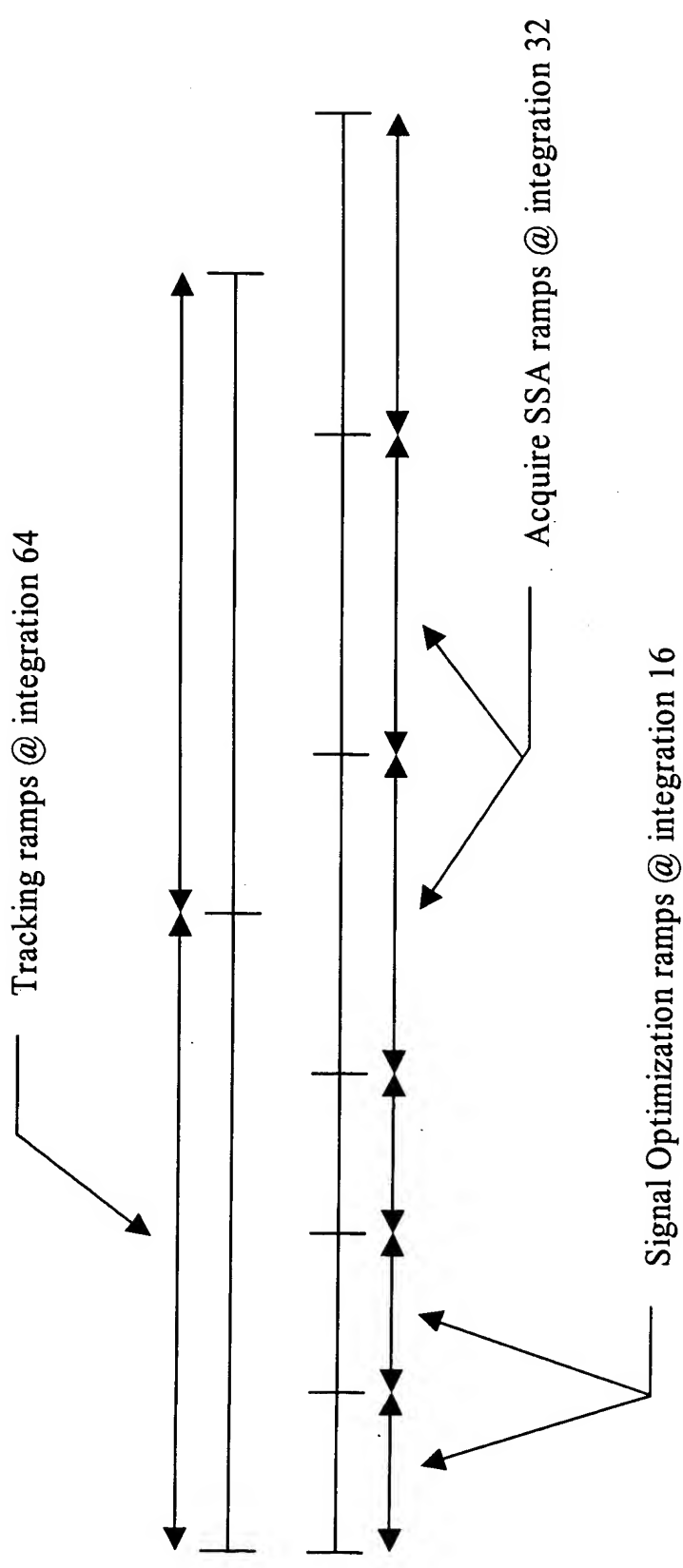


FIG. 48

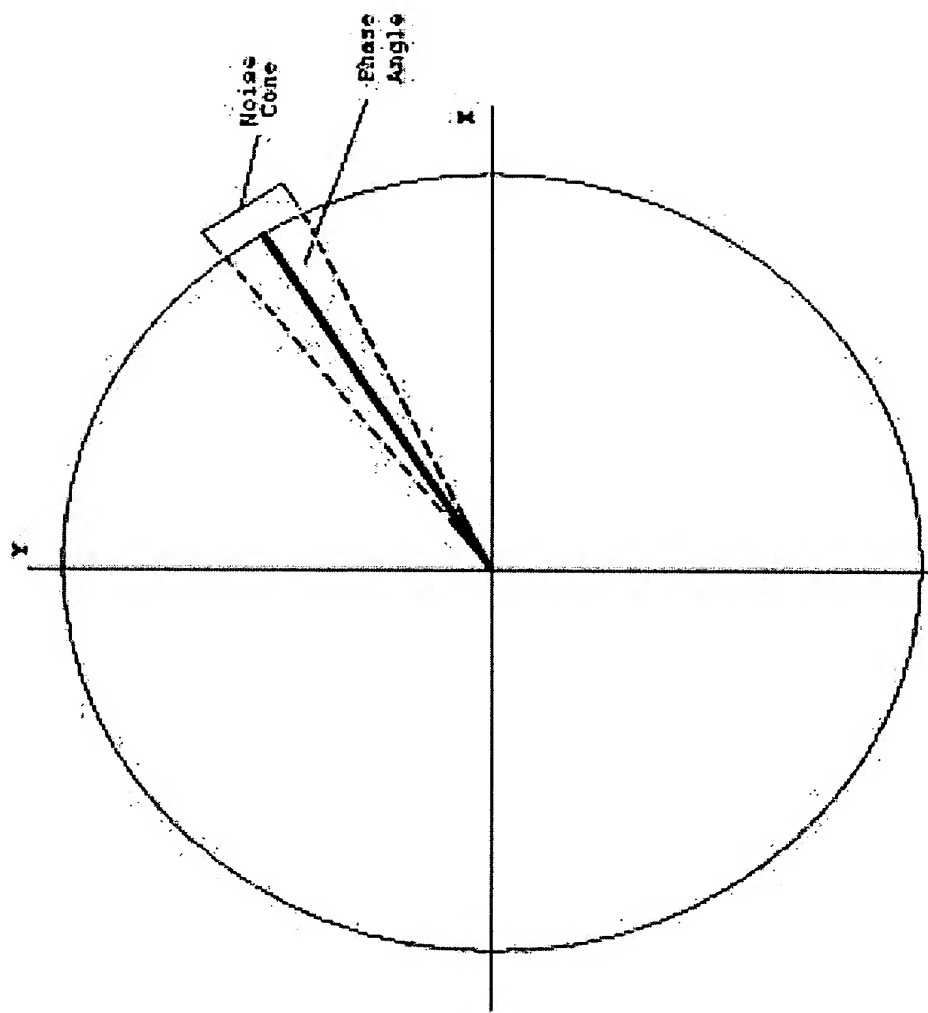


FIG. 49

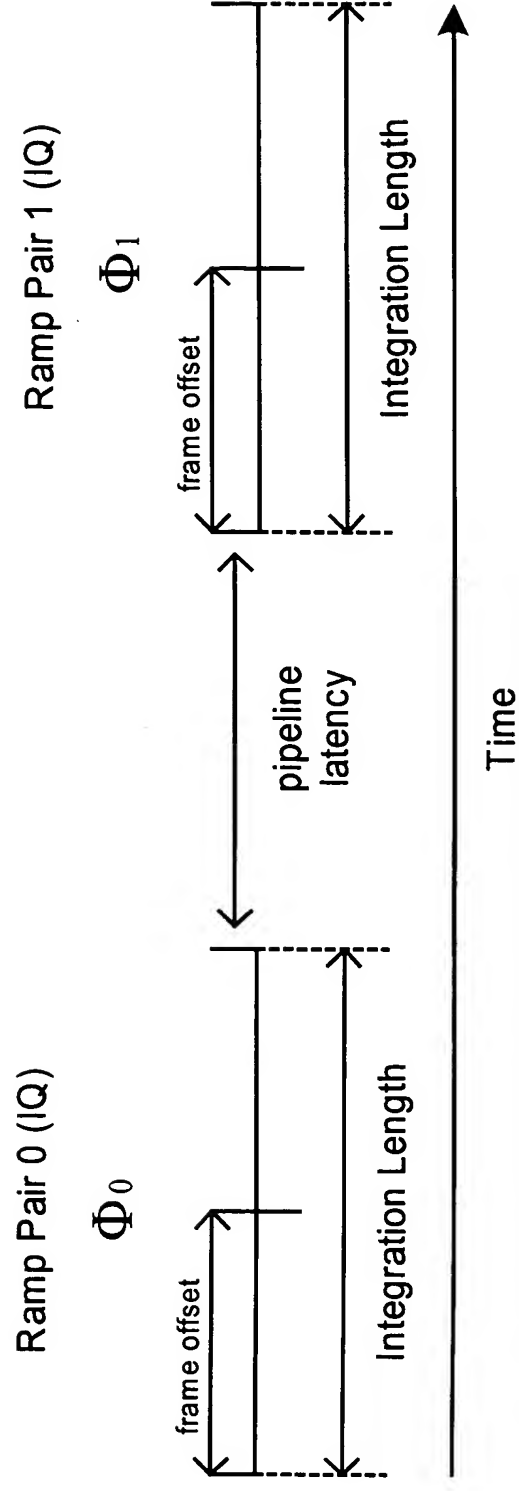
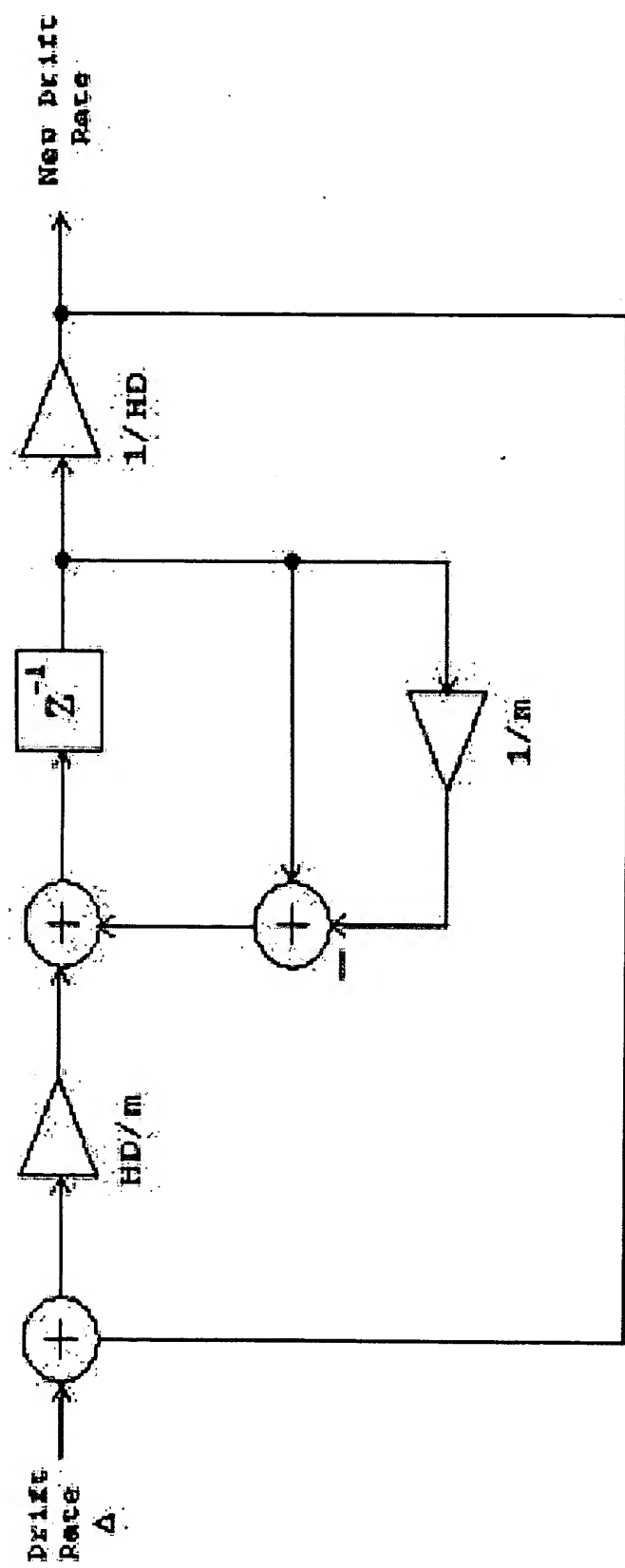


FIG. 50



History Loop

FIG. 51

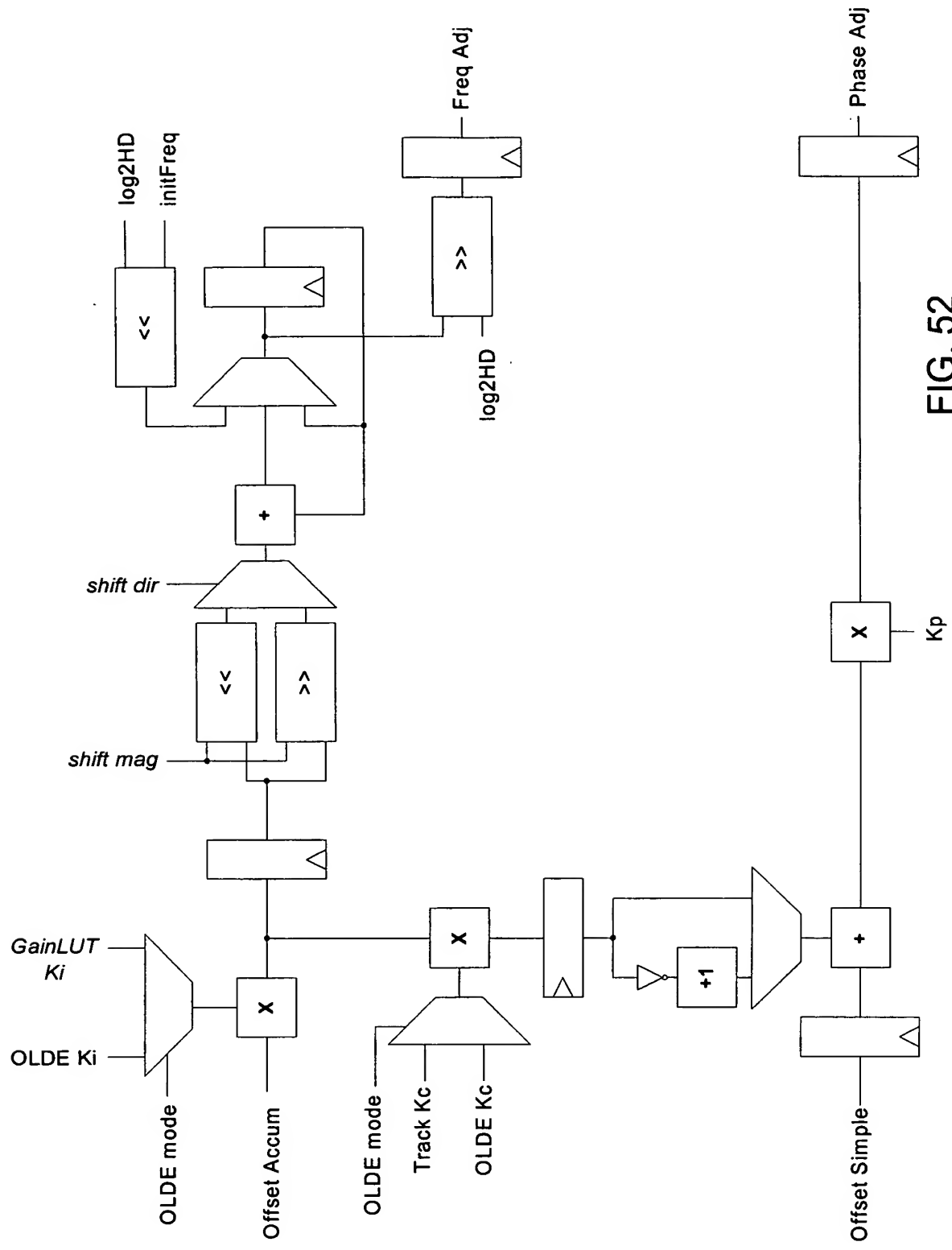


FIG. 52

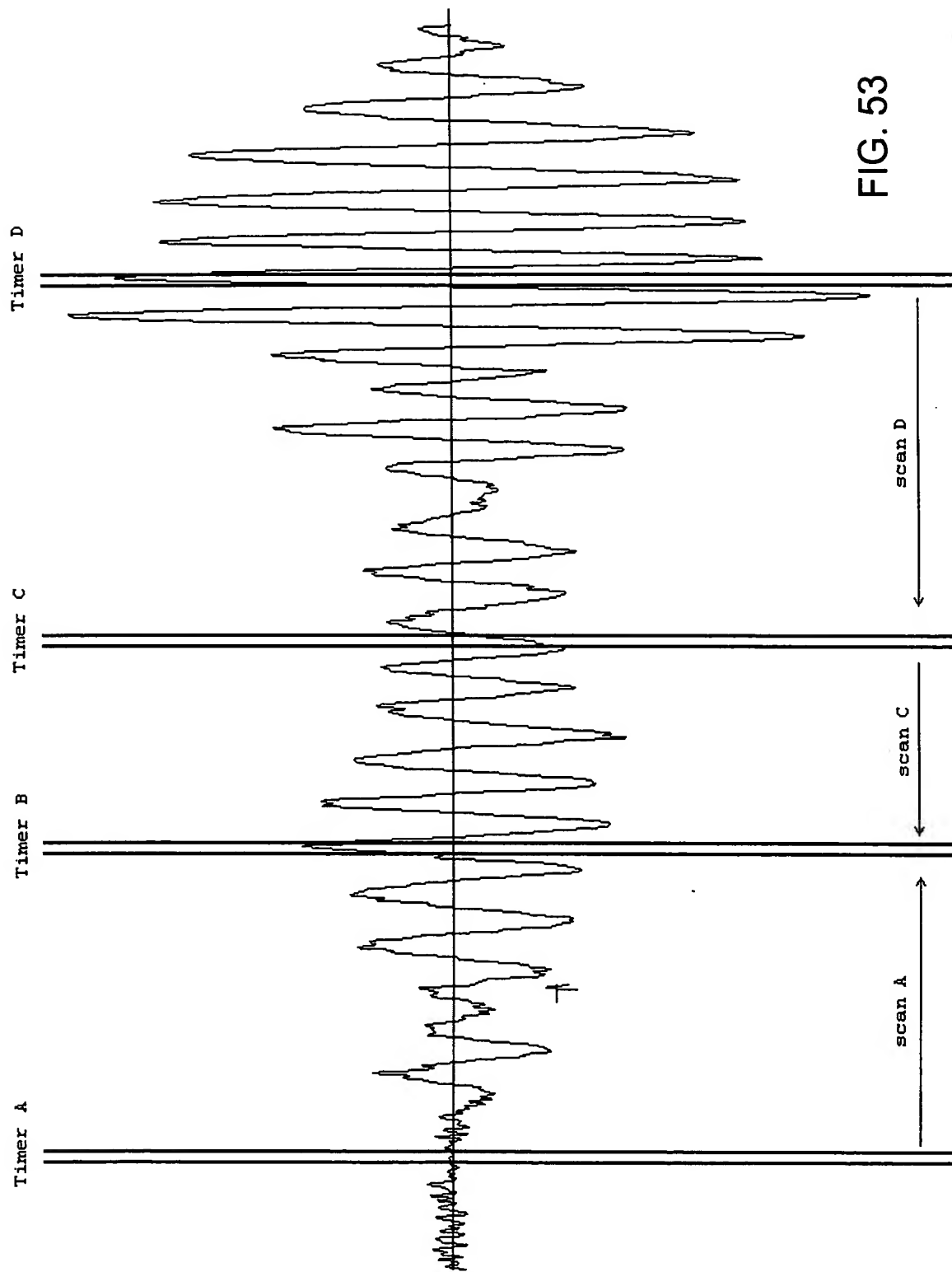


FIG. 53

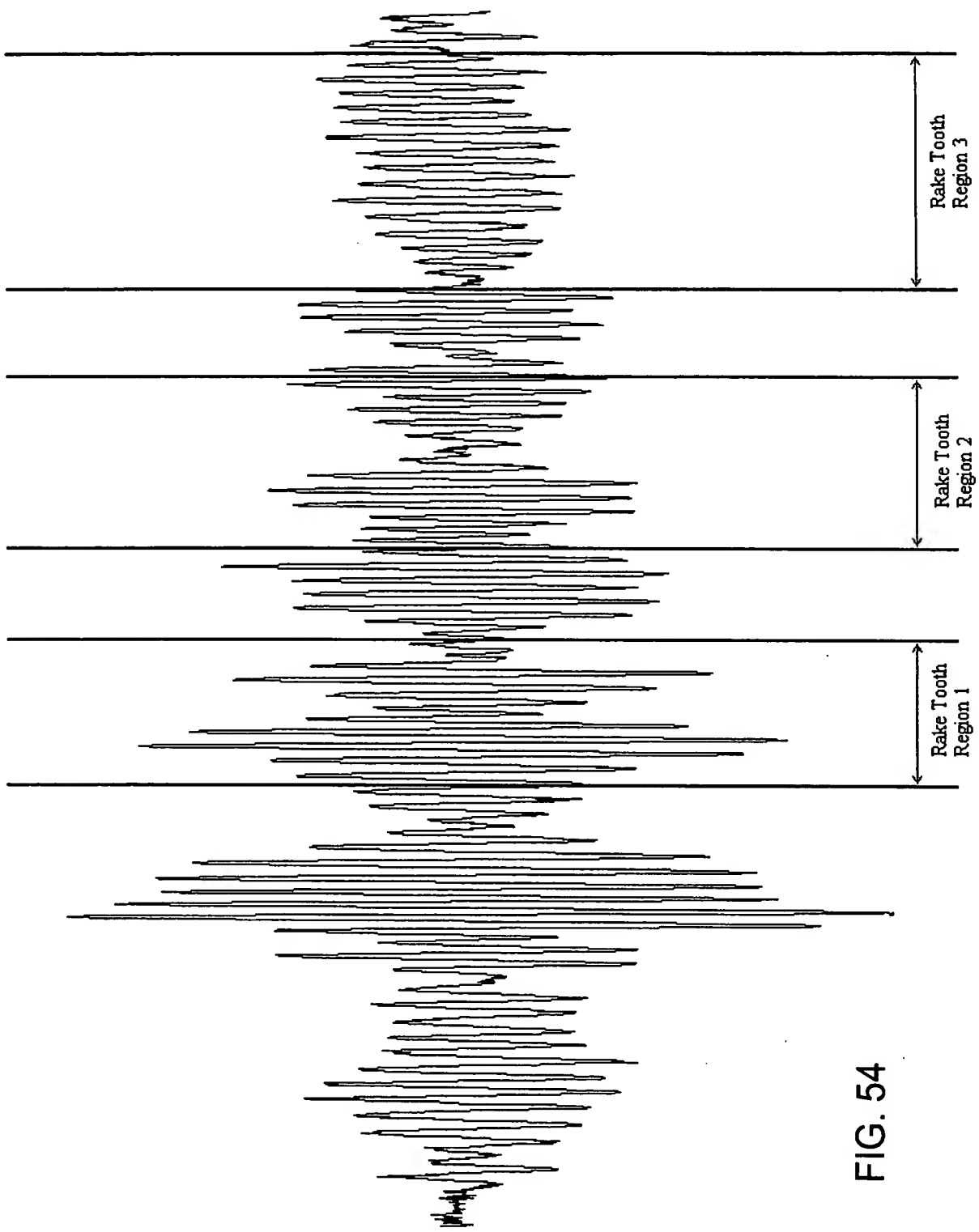


FIG. 54

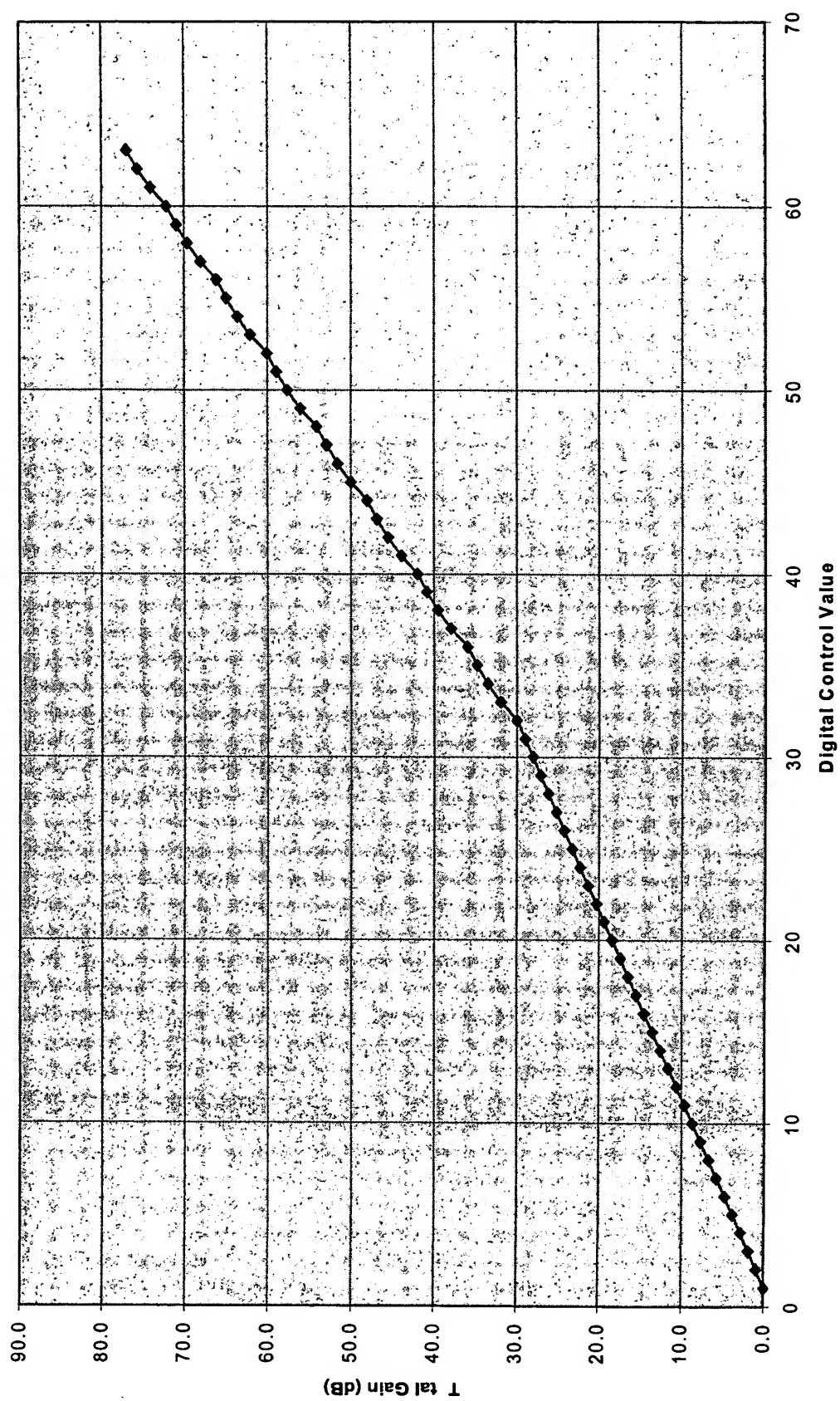


FIG. 55

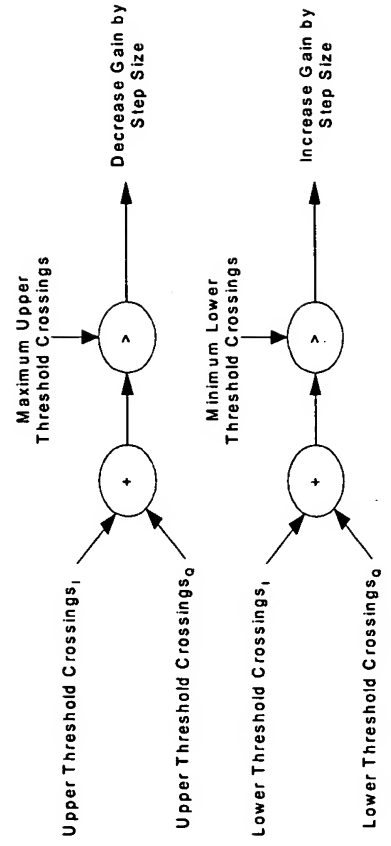
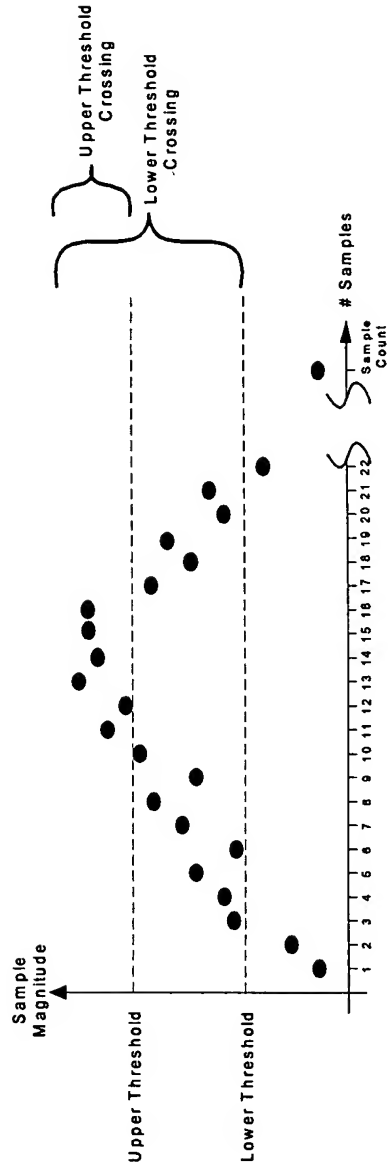
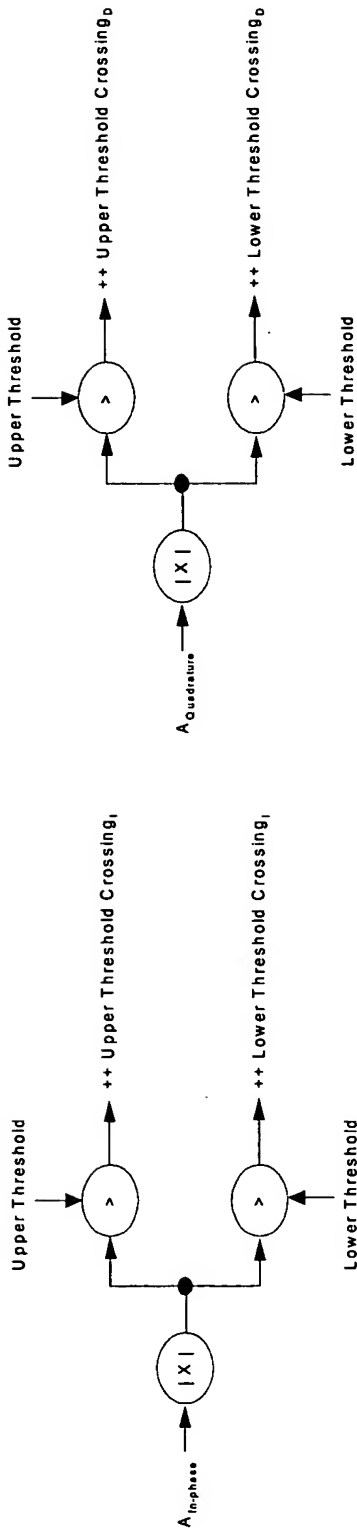


FIG. 56

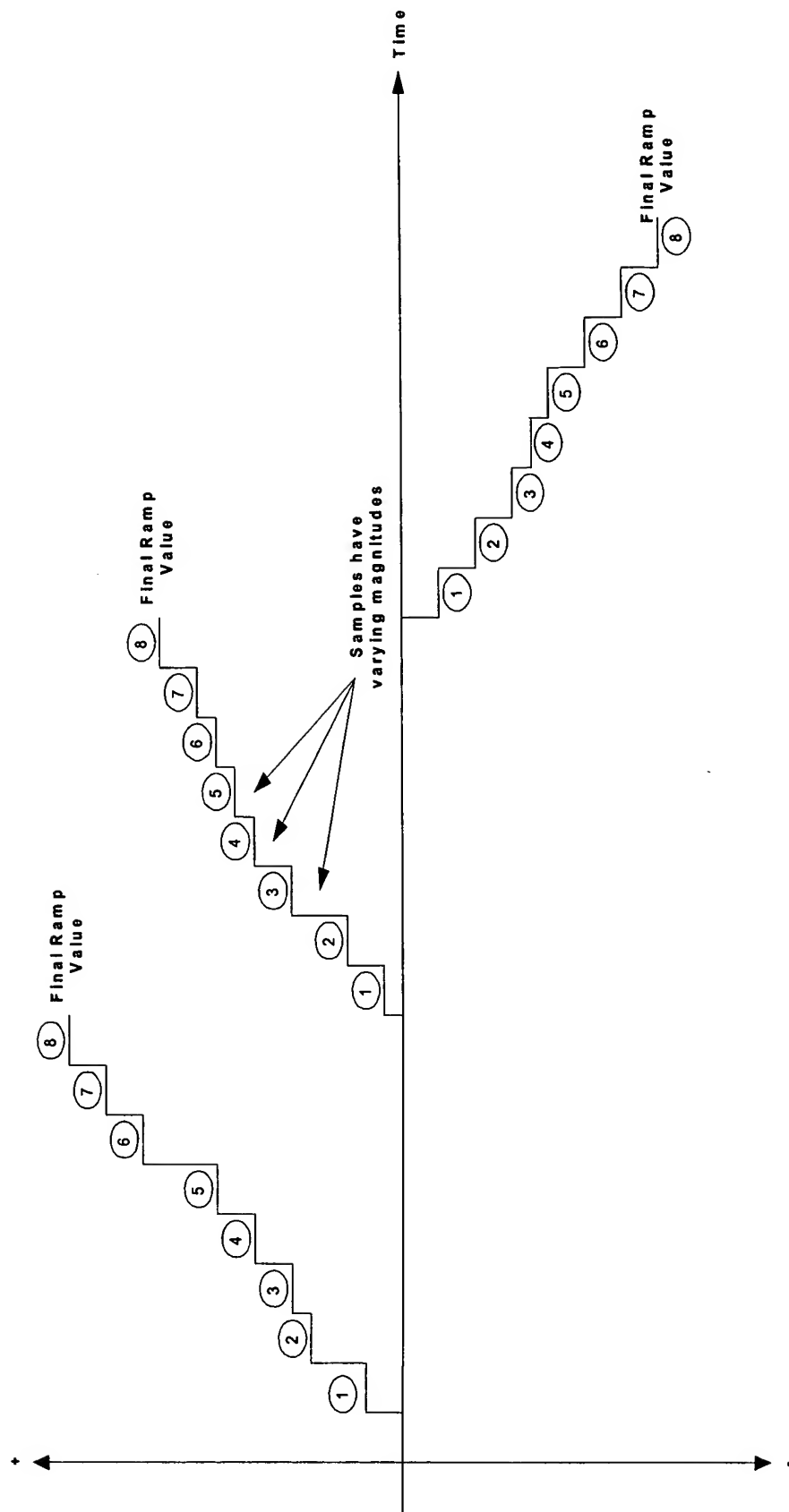


FIG. 57

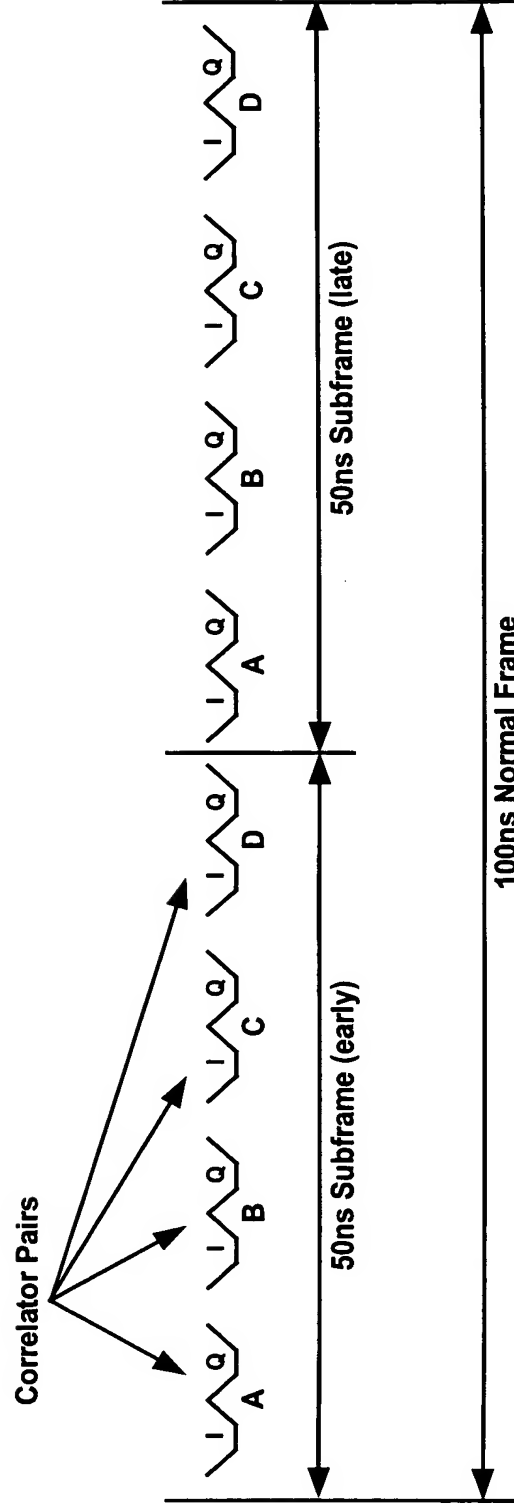


FIG. 58

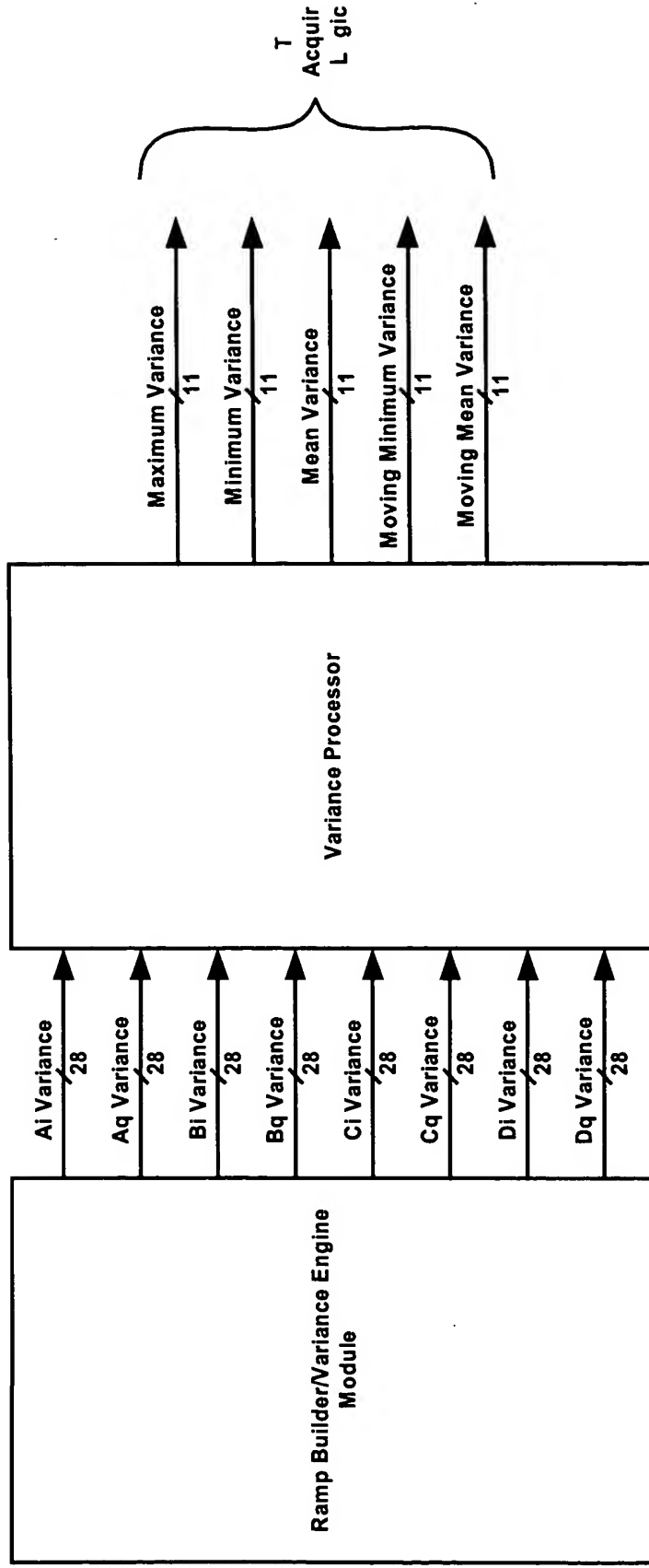


FIG. 59

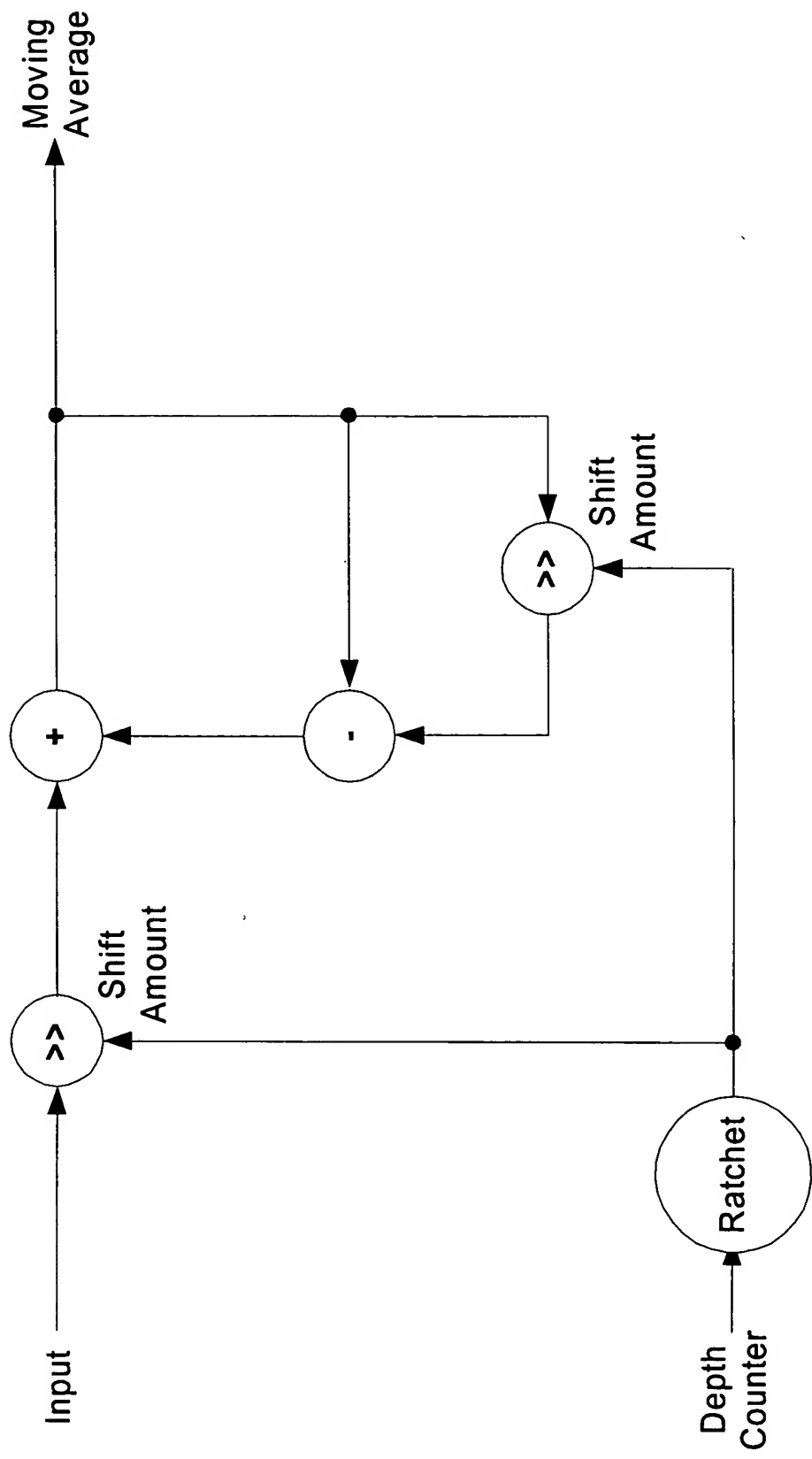


FIG. 60

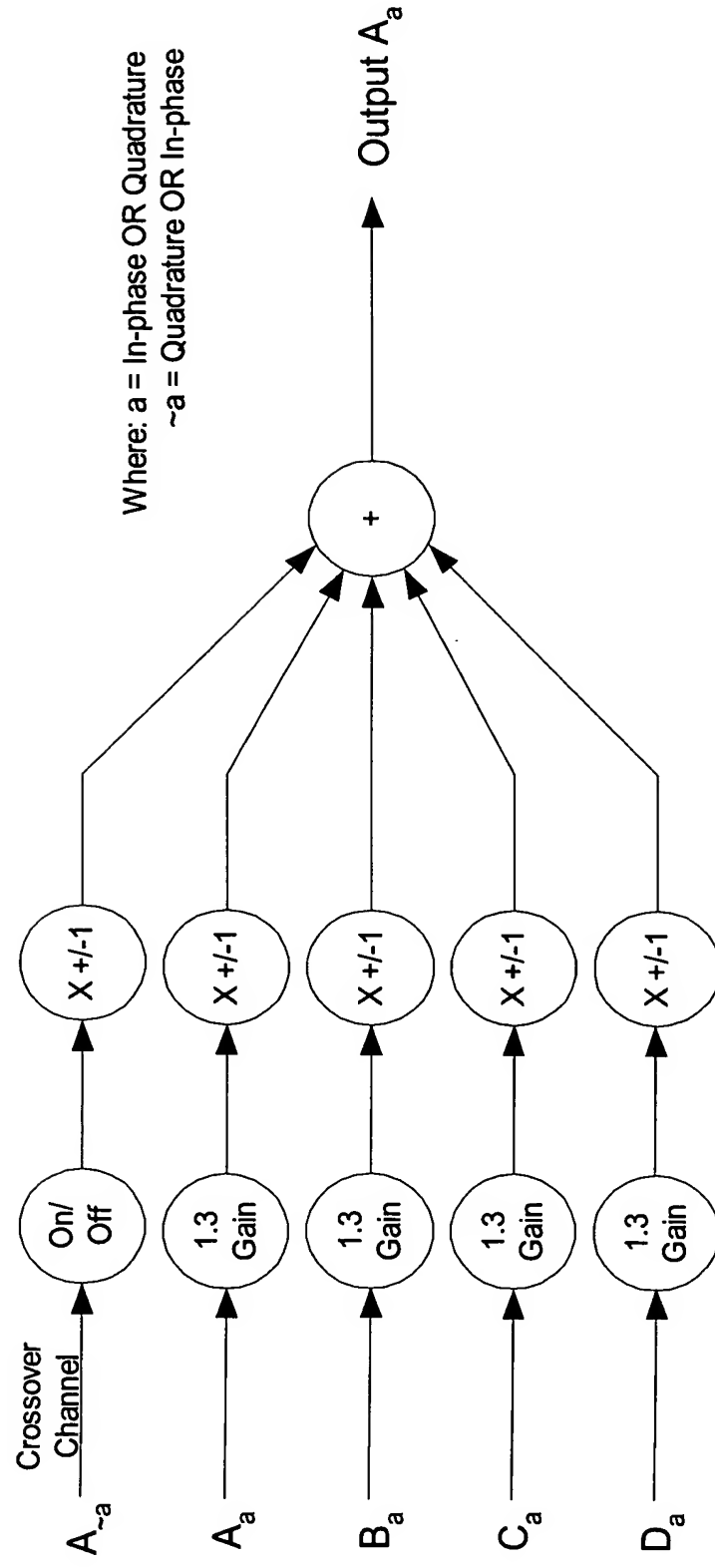
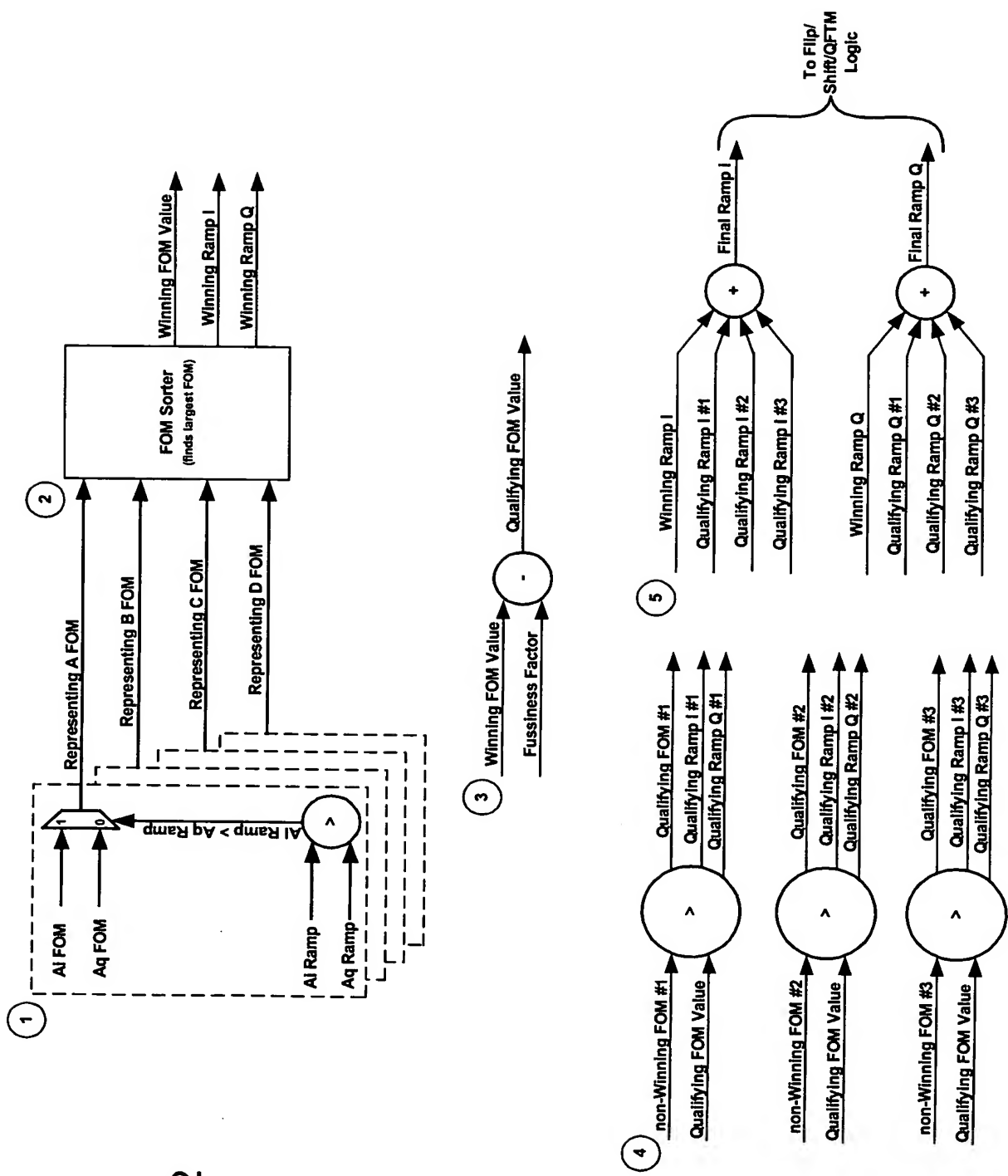


FIG. 61

FIG. 62



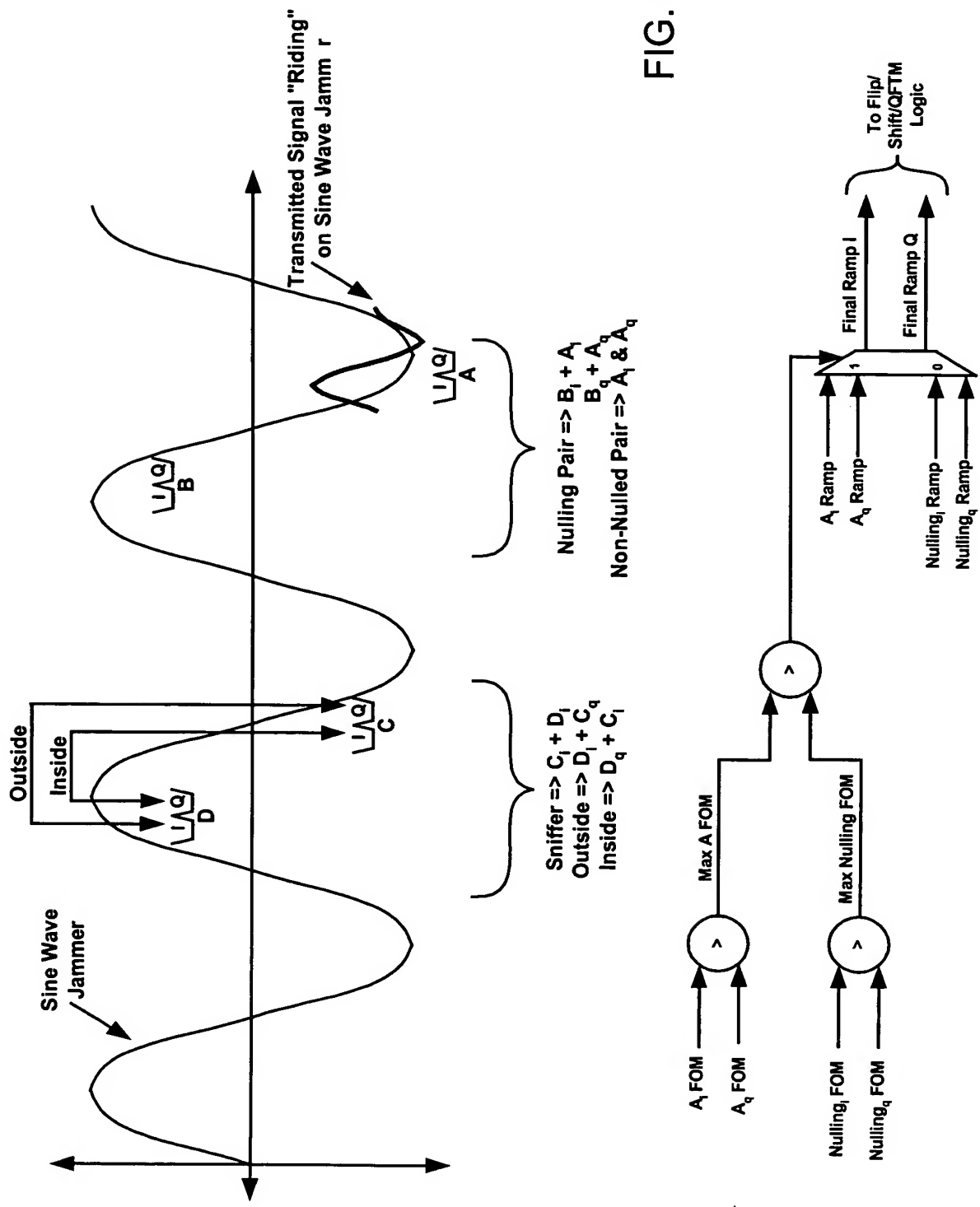


FIG. 63

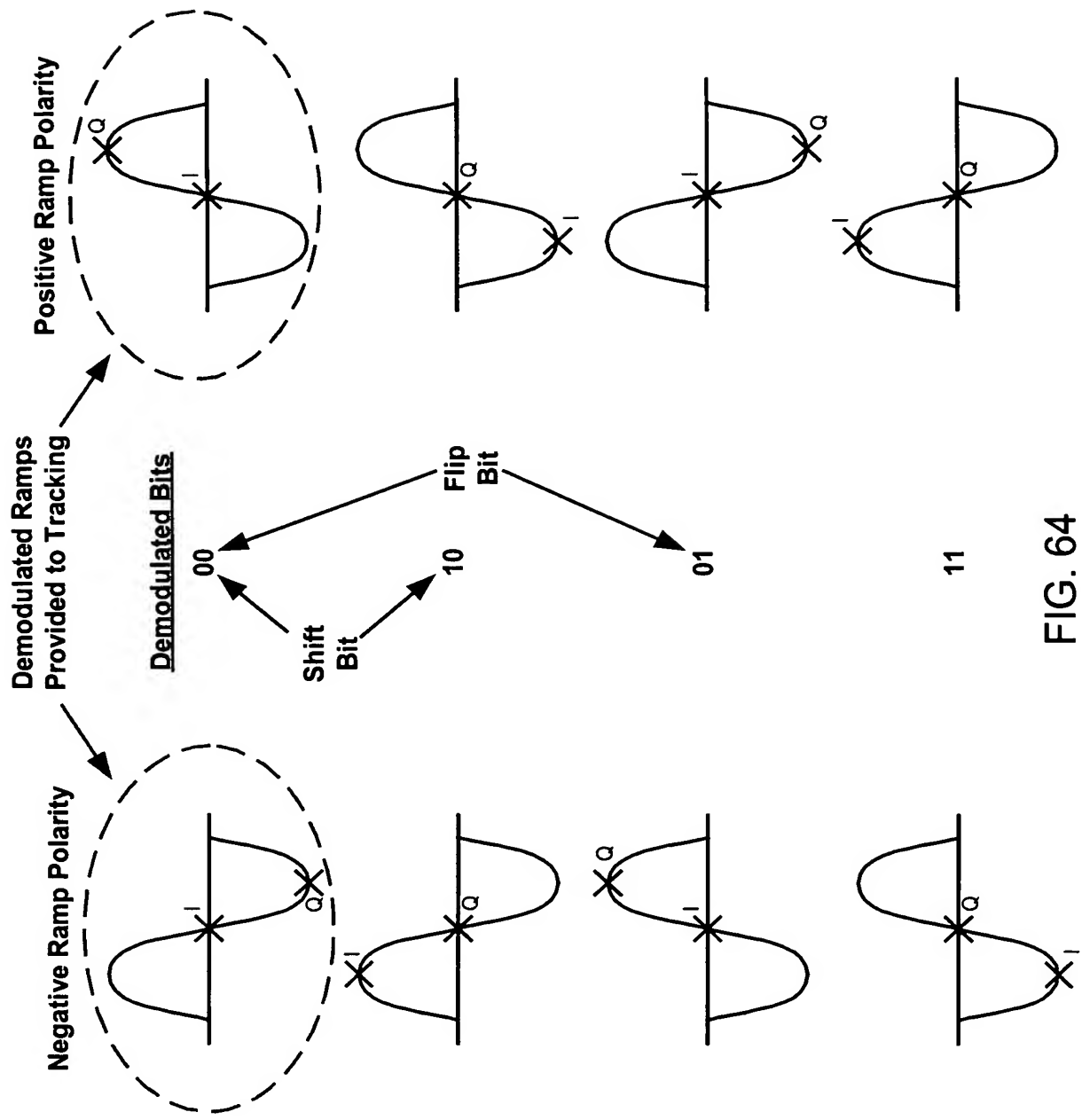


FIG. 64

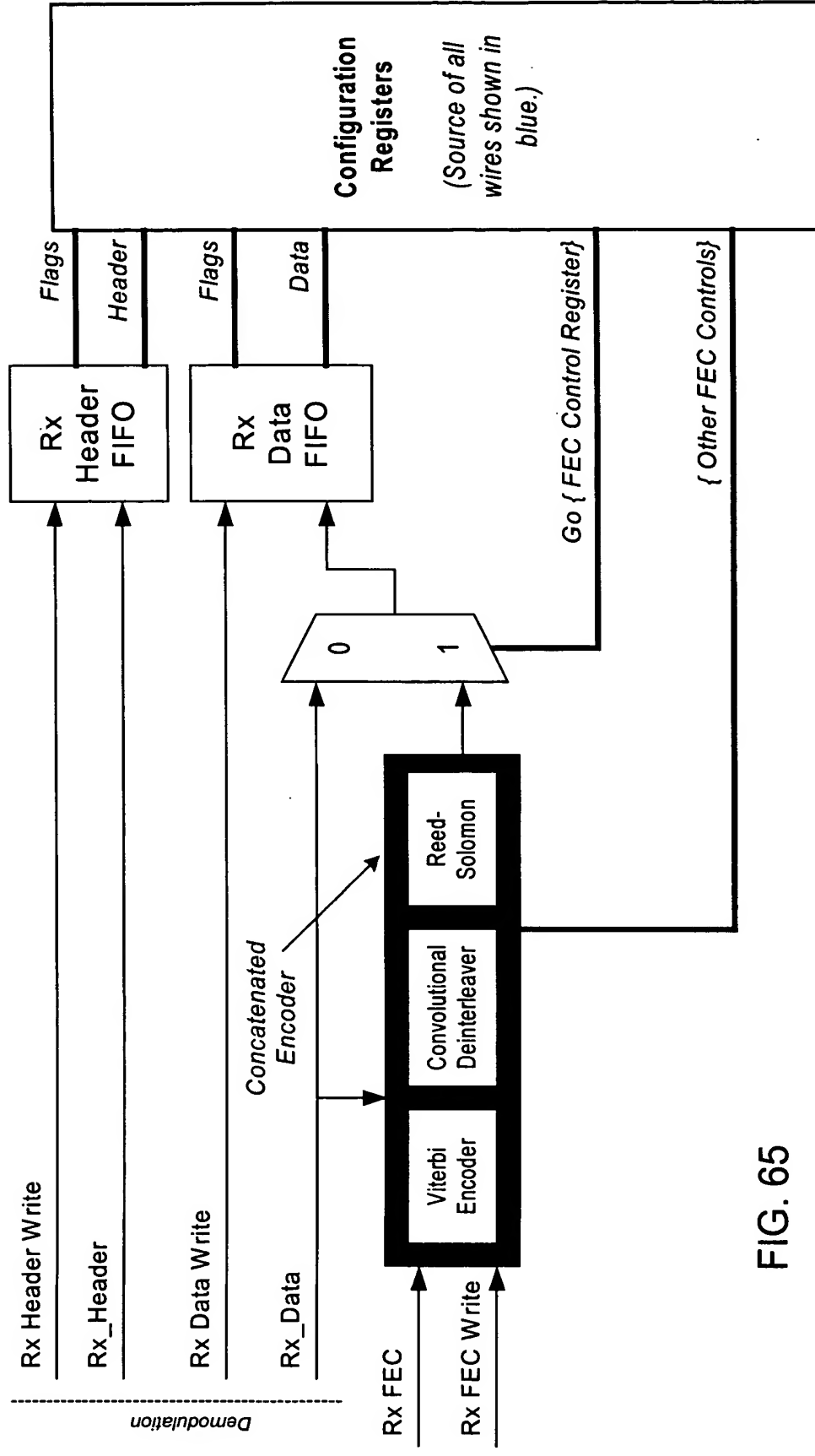


FIG. 65

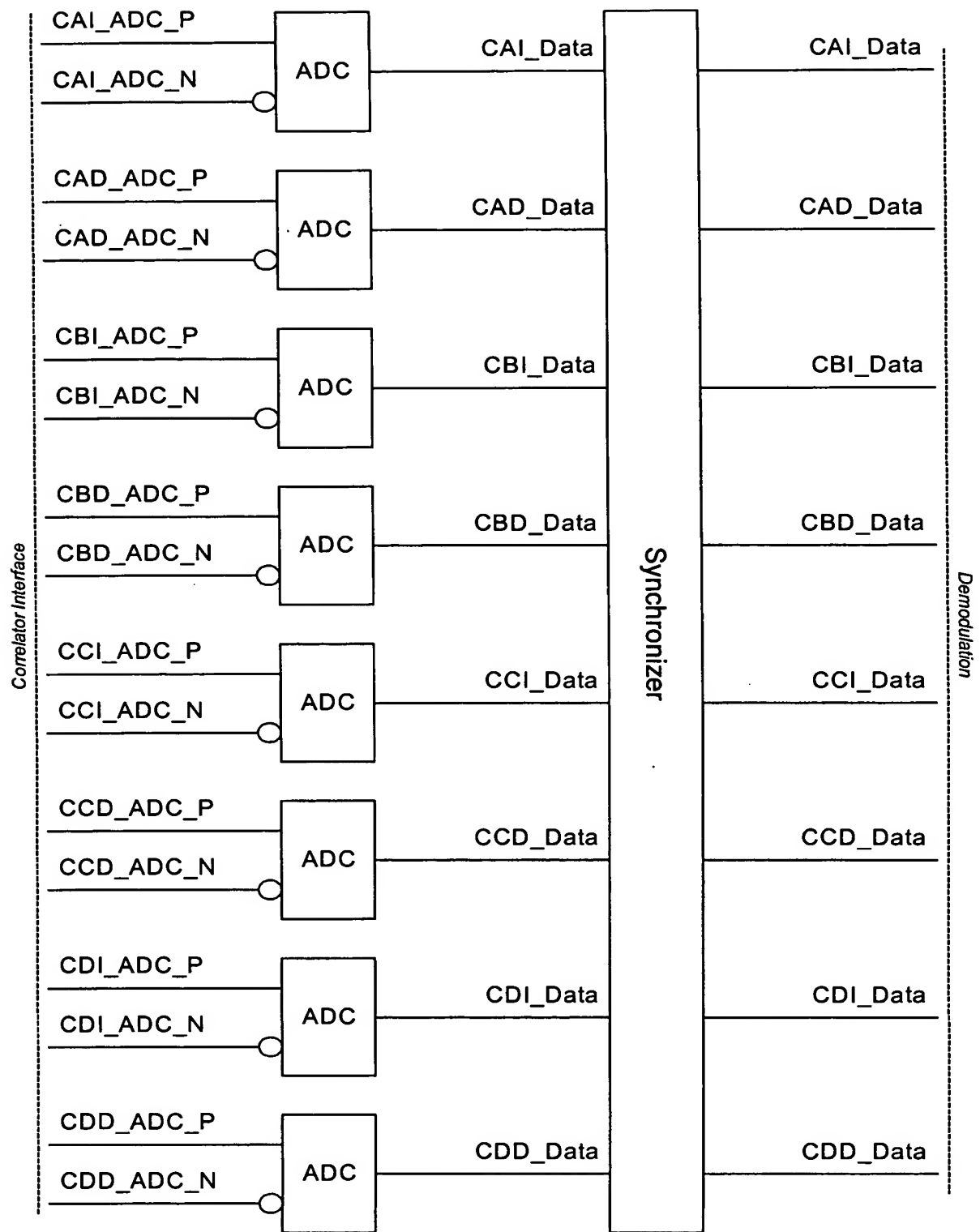


FIG. 66

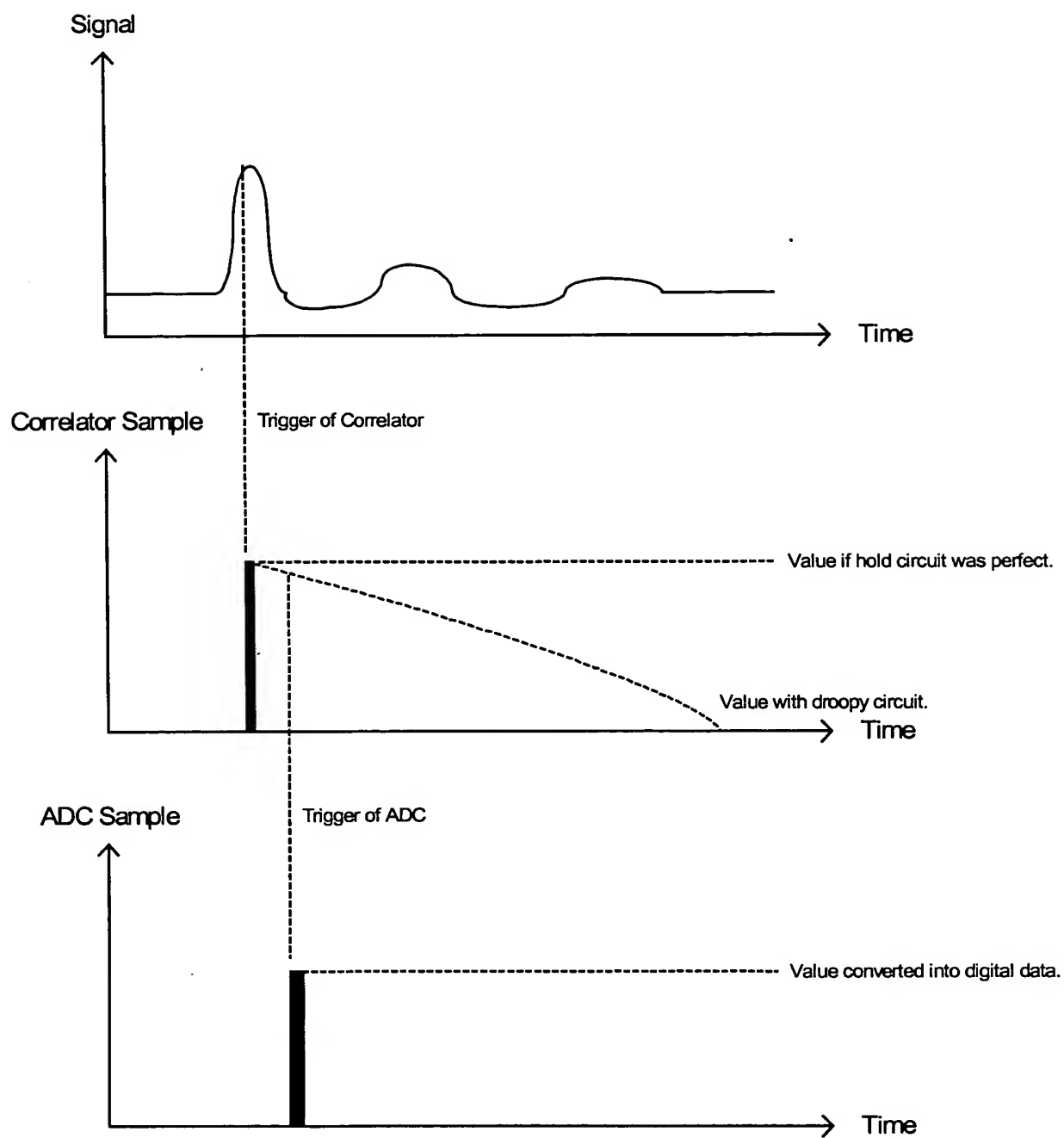
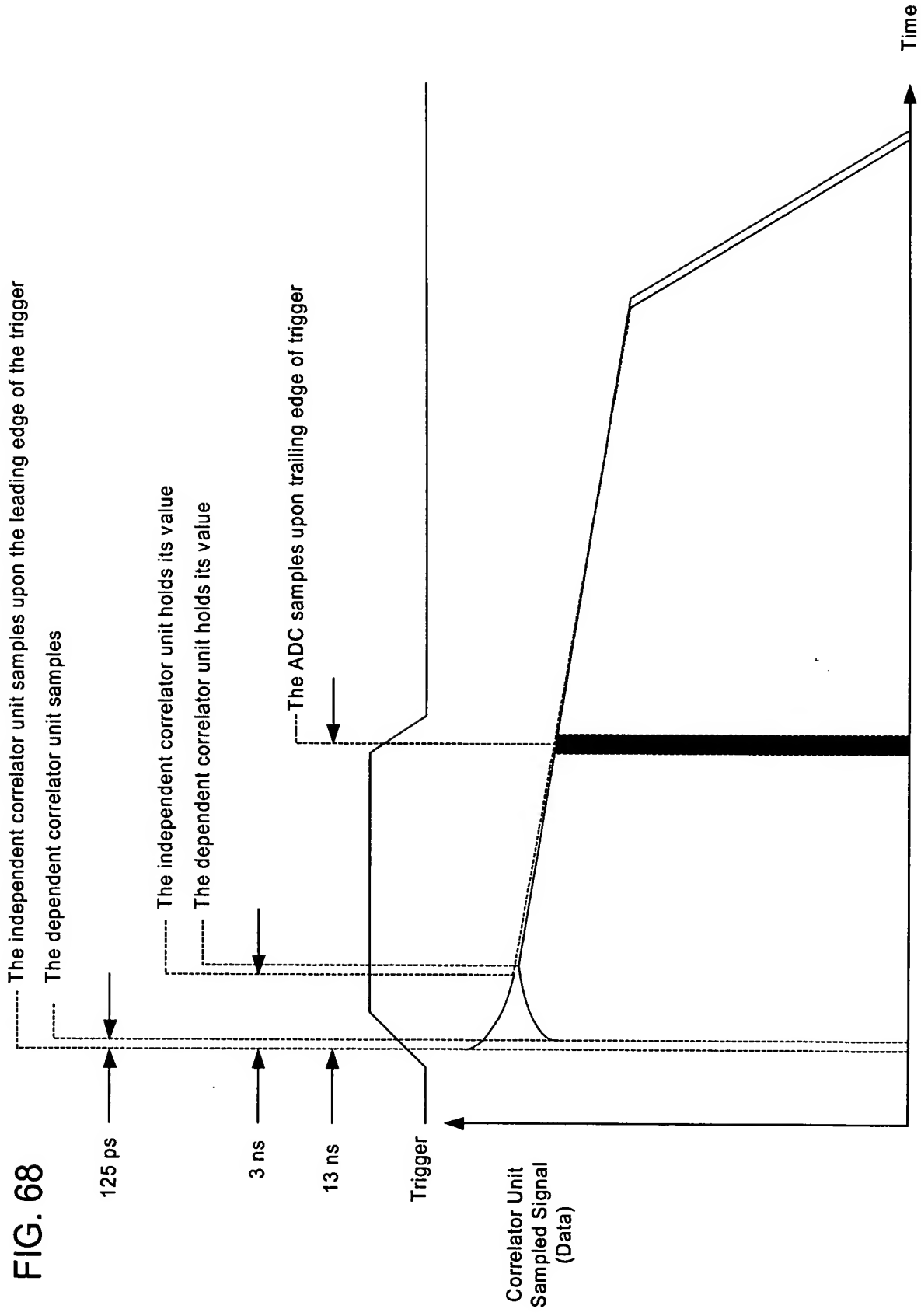


FIG. 67

FIG. 68



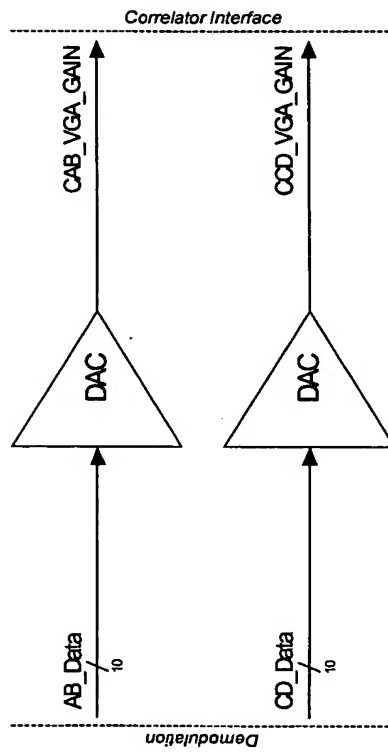


FIG. 69